1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,WHITE_ARROW,MLB,K18

02/01/10

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	MASTER	MASTER
2	2	System Block Diagram	K17_REF	06/30/2009
3	3	Power Block Diagram	K17_REF	06/30/2009
4	4	Revision History	MASTER	MASTER
5	5	BOM Configuration	K17_REF	05/28/2009
6	7	Functional / ICT Test	MASTER	MASTER
7	8	Power Aliases	MASTER	MASTER
8	9	Signal Aliases	K17_REF	06/11/2009
9	10	CPU DMI/PEG/FDI/RSVD	K17_REF	06/15/2009
10	11	CPU Clock/Misc/JTAG	K17_REF	06/15/2009
11	12	CPU DDR3 Interfaces	K17_REF	06/15/2009
12	13	CPU Power (1 of 2)	K17_REF	06/15/2009
13	14	CPU Power (2 of 2)	K17_REF	06/15/2009
14	15	CPU Grounds	K17_REF	06/15/2009
15	16	CPU Non-GFX Decoupling (1 of 2)	K17_REF	06/15/2009
16	17	CPU Non-GFX Decoupling (2 of 2)	K17_REF	06/15/2009
17	18	PCH SATA/PCIE/CLK/LPC/SPI	K17_REF	08/24/2009
18	19	PCH DMI/FDI/Graphics	K17_REF	06/15/2009
19	20	PCH PCI/FlashCache/USB	K18_MLB	10/07/2009
20	21	PCH MISC	K17_REF	06/15/2009
21	22	PCH Power	K17_REF	06/15/2009
22	23	PCH Grounds	K17_REF	06/15/2009
23	24	PCH Non-GFX Decoupling	K17_REF	06/15/2009
24	25	CPU/PCH GFX Decoupling	K17_REF	06/15/2009
25	26	eXtended Debug Port (XDP)	K17_REF	06/15/2009
26	27	Clock (CK505)	K17_MLB	06/23/2009
27	28	Chipset Support	K17_REF	06/15/2009
28	29	DDR3 SO-DIMM Connector A	MASTER	MASTER
29	30	DDR3 Byte/Bit Swaps	MASTER	MASTER
30	31	DDR3 SO-DIMM Connector B	MASTER	MASTER
31	32	CPU Memory S3 Support	K17_REF	06/15/2009
32	33	FSB/DDR3/FRAMEBUF Vref Margining	K17_REF	06/15/2009
33	34	X16/ALS/CAMERA CONNECTOR	K18_COMMS	06/15/2009
34	35	SecureDigital Card Reader	T27_REF	08/26/2009
35	36	USB HUB 1	K18_MLB	10/07/2009
36	37	USB HUB 2	K23F	10/06/2009
37	39	Ethernet PHY (Caesar II/IV)	T27_REF	08/20/2009
38	40	Ethernet Connector	K17_REF	06/15/2009
39	41	FireWire LLC/PHY (FW643)	K19_MLB	05/29/2009
40	42	FireWire Port Power	K19_MLB	05/29/2009
41	43	FireWire Ports	K19_MLB	05/29/2009
42	45	SATA Connectors	T27_REF	10/01/2009
43	46	External USB Connectors	K17_REF	06/15/2009
44	48	Front Flex Support	K19_MLB	05/29/2009
45	49	SMC	K17_REF	06/15/2009
46	50	SMC Support	K18_SENSORS	06/29/2009
47	51	LPC+SPI Debug Connector	K17_MLB	06/23/2009
48	52	K18 SMBus Connections	K18_SENSORS	06/18/2009
49	53	Current & Voltage Sensing	K18_SENSORS	06/29/2009
50	54	Current Sensing	K18_SENSORS	07/02/2009
51	55	Thermal Sensors	K18_SENSORS	06/18/2009
52	56	Fan Connectors	K19_MLB	05/29/2009
53	57	WELLSPRING 1	K19_MLB	05/29/2009
54	58	WELLSPRING 2	K19_MLB	05/29/2009
55	59	Sudden Motion Sensor (SMS)	K19_MLB	05/29/2009
56	60	DEBUG SENSORS AND ADC	K18_SENSORS	07/07/2009
57	61	SPI ROM	K17_REF	06/15/2009
58	62	AUDIO: CODEC/REGULATOR	K18_AUDIO	09/21/2009
59	63	AUDIO: LINE INPUT FILTER	K18_AUDIO	07/29/2009
60	65	AUDIO: HEADPHONE FILTER	K18_AUDIO	07/29/2009
61	66	AUDIO: SPEAKER AMP	K18_AUDIO	07/29/2009
62	67	AUDIO: JACKS	K18_AUDIO	07/29/2009
63	68	AUDIO: JACK TRANSLATORS	K18_AUDIO	07/29/2009
64	69	DC-In & Battery Connectors	K18_POWER	06/30/2009
65	70	PBus Supply & Battery Charger	K18_POWER	06/30/2009
66	72	5V / 3.3V Power Supply	K18_POWER	07/13/2009
67	73	1.5V DDR3 Supply	K18_POWER	07/14/2009
68	74	CPU IMVP VCore Regulator	K18_POWER	06/29/2009
69	75	GFX IMVP VCore Regulator	K18_POWER	07/08/2009
70	76	CPUVTT (1.05V) Power Supply	K18_POWER	07/14/2009
71	77	Misc Power Supplies	K18_POWER	06/29/2009
72	78	Power FETs	K18_POWER	06/10/2009
73	79	Power Control	K17_REF	06/15/2009
74	80	NV GT216 PCI-E	K17_REF	06/15/2009
75	81	NV GT216 CORE/FB POWER	K17_REF	06/15/2009
76	82	NV GT216 FRAME BUFFER I/F	K17_REF	06/15/2009
77	84	GDDR3 Frame Buffer A (Top)	K17_REF	06/15/2009
78	85	GDDR3 Frame Buffer B (Top)	K17_REF	06/15/2009
79	86	NV GT216 GPIO/MIO/MISC	K17_REF	06/15/2009
80	87	GT216 GPIOS & STRAPS	K17_REF	06/15/2009
81	88	NV GT216 VIDEO INTERFACES	K17_REF	06/15/2009
82	89	GPU (GT216) CORE SUPPLY	K18_POWER	07/14/2009
83	90	LVDS Display Connector	K19_MLB	05/29/2009
84	93	Muxed Graphics Support	K17_REF	06/15/2009
85	94	DisplayPort Connector	K17_REF	06/15/2009
86	95	1V8 / 1V55 FB Power Supply	K18_POWER	06/26/2009
87	96	Graphics MUX (GMUX)	K17_REF	06/15/2009
88	97	LCD BACKLIGHT DRIVER	K18_BKLT	07/29/2009
89	98	LCD Backlight Support	K19_MLB	05/29/2009
90	99	Misc Power Supplies	K18_POWER	06/10/2009
91	100	CPU Constraints	K17_REF	06/15/2009
92	101	Memory Constraints	K17_REF	06/15/2009
93	102	PCH Constraints 1	K17_REF	06/15/2009
94	103	PCH Constraints 2	K17_REF	06/15/2009
95	104	Ethernet Constraints	K17_REF	06/15/2009
96	105	FireWire Constraints	K17_REF	06/15/2009
97	106	SMC Constraints	K17_REF	06/15/2009
98	107	GPU (GT216) CONSTRAINTS	K17_REF	06/15/2009
99	108	Project Specific Constraints	K17_REF	06/15/2009
100	109	PCB Rule Definitions	K17_REF	06/15/2009
101	132	BluRay Decrypter Card Connector	K17_REF	06/15/2009

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8504	1	SCHEM,WHITE_ARROW,MLB,K18	SCH	CRITICAL	
820-2850	1	PCBF,WHITE_ARROW,MLB,K18	PCB	CRITICAL	

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TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 1 10:13:48 2010

DRAWING TITLE
SCHEM,WHITE_ARROW,MLB,K18

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 1 OF 132
SHEET 1 OF 101

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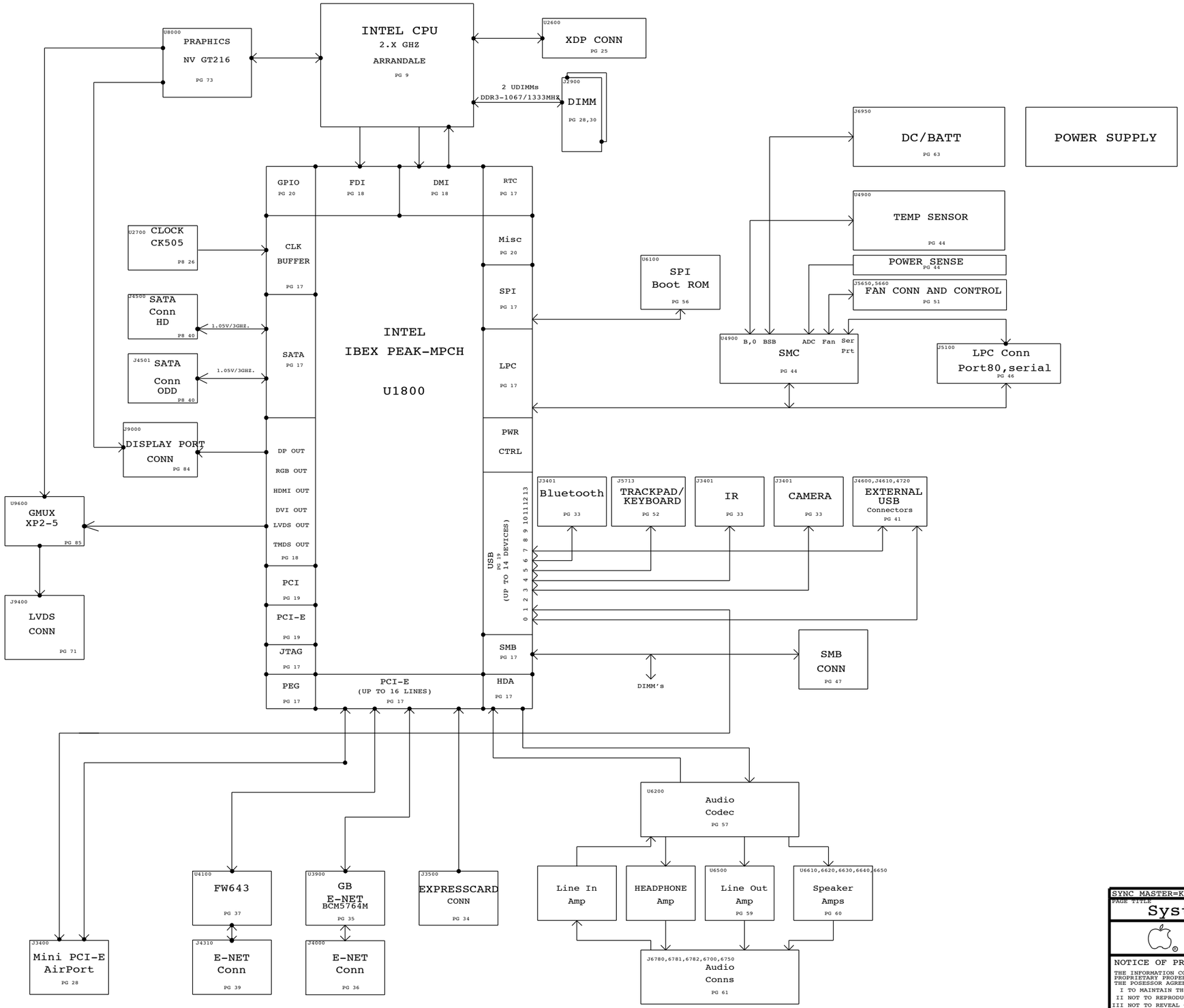

SYNC MASTER=K17 REF SYNC DATE=06/30/2009

PAGE TITLE

System Block Diagram

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DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 2 OF 132

SHEET 2 OF 101

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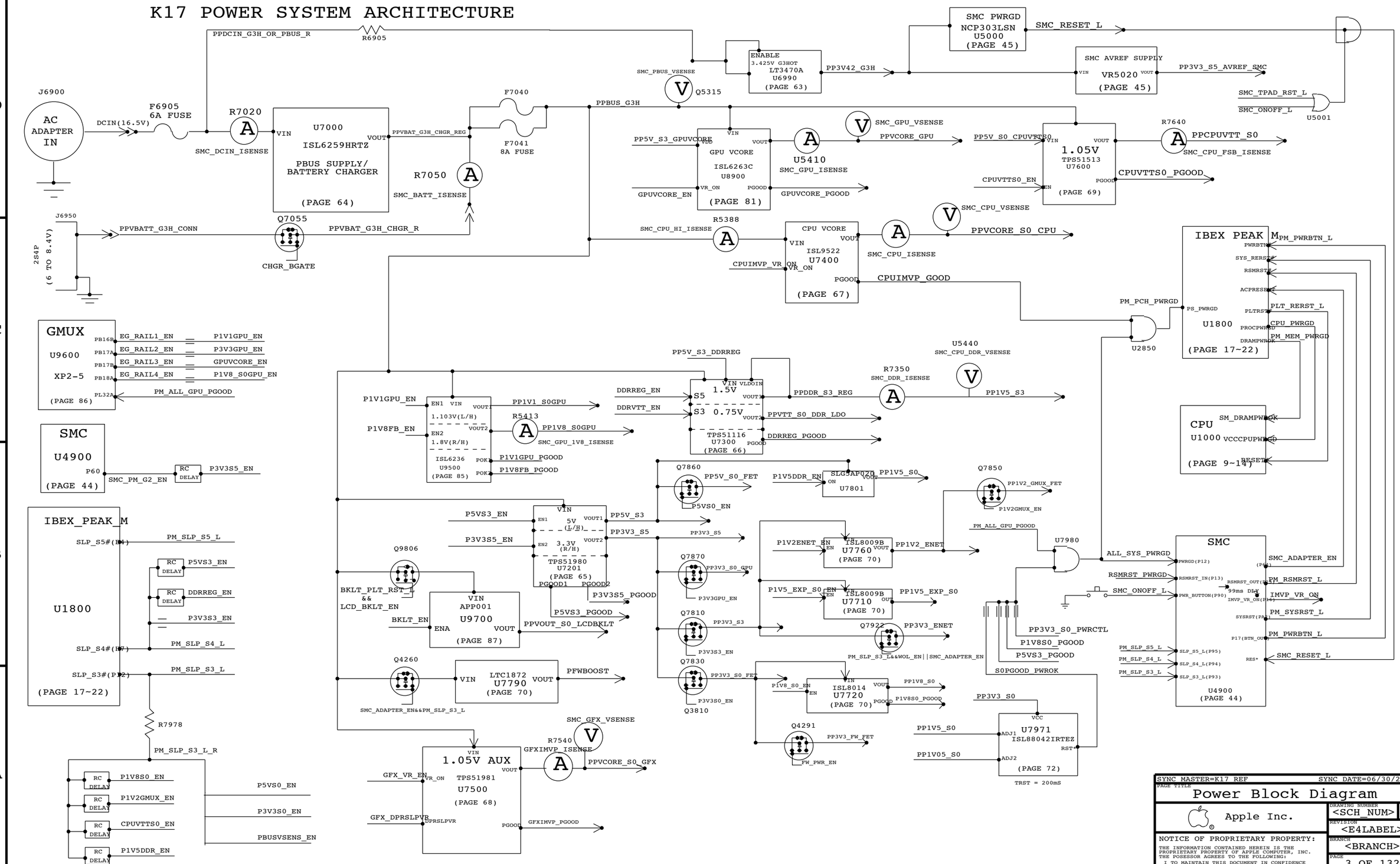
K17 POWER SYSTEM ARCHITECTURE



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PAGE TITLE

Power Block Diagram

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REVISION <E4LABEL>

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PAGE 3 OF 132

SHEET 3 OF 101

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PAGE TITLE

Revision History

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DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 4 OF 132

SHEET 4 OF 101

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0952	PCBA,2.0G,512SAM_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG,K18_PVT,EEEE_DCJ7
639-0953	PCBA,2.0G,512HYN_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_HYNIX,K18_PVT,EEEE_DCJ8
639-0954	PCBA,2.13G,512SAM_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJ9
639-0955	PCBA,2.13G,512HYN_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJC
639-0956	PCBA,2.4G,512SAM_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJD
639-0957	PCBA,2.4G,512HYN_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJF
085-1404	K18 DEVELOPMENT BOM	

K18 BOM GROUPS

BOM GROUP	BOM OPTIONS
K18_COMMON	ALTERNATE,COMMON,K18_COMMON1,K18_COMMON2,K18_PROGPARTS,USBHUB_2061,RDRV:8515A2,DCI
K18_COMMON1	BATT_3S,BCM5764M,GL137,CPUPOC_IMAX_40_50,CPUMEM_S0,SMC_EXCARD_NOT,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM
K18_COMMON2	GMUXPLL_3V3,GPU_SS_INT,MIKEY,GPUVID_0P90V,DPMUX_EN_PLD,DP_CA_DET_EG_PLD,DP_ESD,VFRQ_SLPS3,SMC_OSC_YES,RAIL_MON
K18_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM
K18_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG,FB1V55
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX,FB1V55
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG,FB1V35
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX,FB1V35

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ7]	CRITICAL	EEEE_DCJ7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ8]	CRITICAL	EEEE_DCJ8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ9]	CRITICAL	EEEE_DCJ9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJC]	CRITICAL	EEEE_DCJC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJD]	CRITICAL	EEEE_DCJD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJF]	CRITICAL	EEEE_DCJF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3848	1	ARD,SLBPE,PRQ,2.66G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3847	1	ARD,SLBPF,PRQ,2.53G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3846	1	ARD,SLBNA,PRQ,2.4G,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IC,PCH,IBEX PEAK-M,SLGZS,PRQ,B3,BGA	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP++,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8x8,64 QFN	U3900	CRITICAL	BCM5764M
341S2731	1	IC,1MBIT,SPI FLASH,K17/K18	U3990	CRITICAL	
338S0753	1	IC,FW643-E2,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0233	1	IC,SMC,K18	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2562	1	IC,EFI ROM,DEVELOPMENT,K18	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,PSOC +W/USB,56PIN,MLF,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2566	1	IC,CPLD,LATTICE,132CSBGA,K18	U9600	CRITICAL	GMUX_PROG
333S0507	4	IC,SGRAM,GDDR3,16MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SDRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0533	4	IC,SGRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1404	1	K18 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
333S0506	333S0535		ALL	Hynix 900M alt to 1000M
516S0805	516S0806		ALL	Molex alt to Foxconn
152S1102	152S1088		ALL	Mag layer alt to Vishay
353S2805	353S2603		ALL	Fairchild wafer option
333S0542	333S0507		ALL	Samsung I die alt to H
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
337S3808	337S3839		ALL	A02 alt to A03 GPU
128S0305	128S0294		ALL	6.3V alt to 11V Sanyo

SYNC MASTER=K17 REF SYNC DATE=05/28/2009

PAGE TITLE

BOM Configuration

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REVISION <E4LABEL>

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PAGE 5 OF 132

SHEET 5 OF 101

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Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
TRUE PP5V_S0 — 70 72 86 88 6 7 23 42 47 52 54 68 69 — 3 TPs per Fan
TRUE FAN_LT_PWM 52
TRUE FAN_LT_TACH 52

J5660 (RIGHT FAN CONN)

TRUE FAN_RT_PWM 52
TRUE FAN_RT_TACH 52
TRUE GND — 5 TPs per Fan

J6780 (MIC CONN)

155 TRUE BI_MIC_N 62 63
155 TRUE BI_MIC_SHIELD 62 63
155 TRUE BI_MIC_P 62 63

J6781 & J6782 (SPEAKERS CONN)

199 TRUE SPKRCONN_L_OUT_P 61 62 99
199 TRUE SPKRCONN_L_OUT_N 61 62 99
199 TRUE SPKRCONN_R_OUT_P 61 62 99
199 TRUE SPKRCONN_R_OUT_N 61 62 99
199 TRUE SPKRCONN_S_OUT_P 61 62 99
199 TRUE SPKRCONN_S_OUT_N 61 62 99

J9000 (LVDS CONN)

199 TRUE PP3V3_SW_LCD 84 85 87 88 99 83
199 TRUE PP3V3_S0 50 51 52 54 59 60 61 62 63 68 69 72 37 38 39 40 41 42 43 44 45 46 47 48 — 73 80 83
199 TRUE PPVOUT_S0_LCDBKLT — 2 TP needed
199 TRUE LVDS_DDC_CLK 83 84
110 TRUE LVDS_DDC_DATA 83 84
110 TRUE LVDS_CONN_A_DATA_P<0> 83 84 98
110 TRUE LVDS_CONN_A_DATA_N<0> 83 84 98
110 TRUE LVDS_CONN_A_DATA_P<1> 83 84 98
110 TRUE LVDS_CONN_A_DATA_N<1> 83 84 98
110 TRUE LVDS_CONN_A_DATA_P<2> 83 84 98
110 TRUE LVDS_CONN_A_DATA_N<2> 83 84 98
110 TRUE LVDS_CONN_A_CLK_F_P 83 98
110 TRUE LVDS_CONN_A_CLK_F_N 83 98
110 TRUE LVDS_CONN_B_DATA_P<0> 83 84 98
110 TRUE LVDS_CONN_B_DATA_N<0> 83 84 98
110 TRUE LVDS_CONN_B_DATA_P<1> 83 84 98
110 TRUE LVDS_CONN_B_DATA_N<1> 83 84 98
110 TRUE LVDS_CONN_B_DATA_P<2> 83 84 98
110 TRUE LVDS_CONN_B_DATA_N<2> 83 84 98
110 TRUE LVDS_CONN_B_CLK_F_P 83 98
110 TRUE LVDS_CONN_B_CLK_F_N 83 98
110 TRUE LED_RETURN_1 83 88
110 TRUE LED_RETURN_2 83 88
110 TRUE LED_RETURN_3 83 88
110 TRUE LED_RETURN_4 83 88
110 TRUE LED_RETURN_5 83 88
110 TRUE LED_RETURN_6 83 88
TRUE GND — 4 TPs

J4500 (SATA ODD CONN)

110 TRUE PP5V_SW_ODD 42 56 — 3 TPs
110 TRUE SMC_ODD_DETECT 42 45
110 TRUE SATA_ODD_D2R_C_P 42 93
110 TRUE SATA_ODD_D2R_C_N 42 93
110 TRUE SATA_ODD_R2D_P 42 93
110 TRUE SATA_ODD_R2D_N 42 93
TRUE GND — 5 TPs

J4501 (SATA HDD CONN)

110 TRUE PP5V_S0_HDD_FLT 42
110 TRUE SATA_HDD_R2D_P 42 93
110 TRUE SATA_HDD_R2D_N 42 93
110 TRUE SATA_HDD_D2R_C_N 42 93
110 TRUE SATA_HDD_D2R_C_P 42 93
TRUE GND

J5815 (KBD BACKLIGHT CONN)

110 TRUE KBDLED_ANODE 54
110 TRUE SMC_KDBLED_PRESENT_L 54
TRUE GND

FUNC_TEST
TRUE GND
TRUE GND — 6 TPs

USB PORTS

110 TRUE PP5V_S3_RTUSB_A_F 43
110 TRUE USB_LT2_N 43 99
110 TRUE USB_LT2_P 43 99
TRUE GND

110 TRUE PP5V_S3_RTUSB_B_F 43
110 TRUE USB_LT2_N 43 99
110 TRUE USB_LT2_P 43 99
TRUE GND

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

110 TRUE PCIE_AP_D2R_P 17 33 94
110 TRUE PCIE_AP_D2R_N 17 33 94
110 TRUE PCIE_AP_R2D_P 33 94
110 TRUE PCIE_AP_R2D_N 33 94
110 TRUE PCIE_CLK100M_AP_CONN_P 33 99
110 TRUE PCIE_CLK100M_AP_CONN_N 33 99
110 TRUE AP_CLKREQ_O_L 33
110 TRUE PCIE_WAKE_L 18 27 33
110 TRUE AP_RESET_CONN_L 33
110 TRUE PP3V3_WLAN 33
110 TRUE PP5V_S3_ALSCAMERA_F 33
110 TRUE SMBUS_SMC_A_S3_SDA 6 33 45 48 54 97
110 TRUE SMBUS_SMC_A_S3_SCL 6 33 45 48 54 97
110 TRUE USB_CAMERA_CONN_P 33 93
110 TRUE USB_CAMERA_CONN_N 33 93
110 TRUE CONN_USB2_BT_P 33 99
110 TRUE CONN_USB2_BT_N 33 99

J3500 (SD CARD CONN)

145 TRUE SD_D<7..0> 34
145 TRUE SD_CMD 34
145 TRUE SD_CLK 34
145 TRUE SD_CD_L 34 37
145 TRUE SD_WP 34 37
TRUE GND — 2 TPs

J5800 (IPD FLEX CONN)

110 TRUE PP18V5_S3 6 54
112 TRUE Z2_CS_L 53 54
110 TRUE Z2_DEBUG3 53 54
110 TRUE Z2_MISO 53 54
110 TRUE Z2_BOOST_EN 54
110 TRUE Z2_SCLK 53 54
110 TRUE Z2_CLKIN 53 54
110 TRUE Z2_KEY_ACT_L 53 54
110 TRUE Z2_RESET 53 54
110 TRUE PSOC_F_CS_L 53 54
110 TRUE PICKB_L 53 54
110 TRUE PSOC_MISO 53 54
110 TRUE PSOC_MOSI 53 54
110 TRUE PSOC_SCLK 53 54
110 TRUE SMBUS_SMC_A_S3_SCL 6 33 45 48 54 97
110 TRUE SMBUS_SMC_A_S3_SDA 6 33 45 48 54 97

J6900 (DC POWER CONN)

110 TRUE ADAPTER_SENSE 64
110 TRUE PP18V5_DCIN_FUSE 64
TRUE GND

J6950 (MAIN BATT CONN)

110 TRUE PPVBAT_G3H_CONN 64 65
110 TRUE SMBUS_SMC_BSA_SCL 6 45 48 64 65 97
110 TRUE SMBUS_SMC_BSA_SDA 6 45 48 64 65 97
110 TRUE NC_SMC_BS_ALRT_L 6
TRUE GND

J6995 (BAT LED CONN)

110 TRUE PP3V42_G3H 72 64 65 66 46 47 53 55 6 7 17 21 23 43 45 46 47 17 6
110 TRUE SMBUS_SMC_BSA_SDA 6 45 48 64 65 97
110 TRUE SMBUS_SMC_BSA_SCL 6 45 48 64 65 97
110 TRUE SMC_BIL_BUTTON_L 45 46 64
TRUE GND

J5713 (KEY BOARD CONN)

110 TRUE PP3V3_S3 — 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 — 73 87 101 3 17 21 23 43 48 49 50 51 64 65 66 73
110 TRUE PP3V42_G3H 53
110 TRUE WS_KBD1 53
110 TRUE WS_KBD2 53
110 TRUE WS_KBD3 53
110 TRUE WS_KBD4 53
110 TRUE WS_KBD5 53
110 TRUE WS_KBD6 53
110 TRUE WS_KBD7 53
110 TRUE WS_KBD8 53
110 TRUE WS_KBD9 53
110 TRUE WS_KBD10 53
110 TRUE WS_KBD11 53
110 TRUE WS_KBD12 53
110 TRUE WS_KBD13 53
110 TRUE WS_KBD14 53
110 TRUE WS_KBD15_CAP 53
110 TRUE WS_KBD16_NUM 53
110 TRUE WS_KBD17 53
110 TRUE WS_KBD18 53
110 TRUE WS_KBD19 53
110 TRUE WS_KBD20 53
110 TRUE WS_KBD21 53
110 TRUE WS_KBD22 53
110 TRUE WS_KBD23 53
110 TRUE WS_KBD_ONOFF_L 53
110 TRUE WS_LEFT_SHIFT_KBD 53
110 TRUE WS_LEFT_OPTION_KBD 53
110 TRUE WS_CONTROL_KBD 53

J6950 (BIL CABLE CONN)

110 TRUE PP5V_S3_IR_R 42
110 TRUE SMC_LID_R 64
110 TRUE IR_RX_OUT 42 44
110 TRUE SYS_LED_ANODE 42 46
TRUE GND

POWER RAILS

FUNC_TEST
TRUE PM_SLP_S3_L 18 31 45 73 85
TRUE PP0V75_S0_DDRVTT 7 28 30 31 67
TRUE PP18V5_S3 6 54
TRUE PP1V05_S0 7 10 12 13 15 17 18 20 21 23 24 28 34 40 70 73 86
TRUE PP1V05_S0GPU 7 74 76 79 81 86
TRUE PP1V05_S5 7 17 71
TRUE PP1V0_FW_FWPHY 7 39 40
TRUE PP1V2_ENET 7 37 71 72
TRUE PP1V2_S0 7 72 87
TRUE PP1V5_S3 7 28 30 31 67 72
TRUE PP1V5_S3RS0 7 13 16 31 42 72 73 99
TRUE PP1V8R1V55_S0GPU_ISNS 7 8 50 56 75 76 77 78
TRUE PP1V8R1V55_S0GPU_ISNS_R 7 50 86
TRUE PP1V8_GPUIFPX 7 72 81
TRUE PP1V8_S0 7 12 16 21 23 24 58 71 72 87
TRUE PP3V3_ENET 7 27 37 73
TRUE PP3V3_FW_FWPHY 7 39 40 41 — 83 84 85 87 88 99
TRUE PP3V3_S0 50 51 52 54 59 60 61 62 63 68 69 72 6 7 13 14 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48 — 73 80
TRUE PP3V3_S0GPU 7 72 74 79 80 81 82 84 — 73 80
TRUE PP3V3_S3 6 7 8 17 20 31 32 33 34 35 36 48 50 53 54 55 72 73 87 101
TRUE PP3V3_S5 7 17 18 19 20 21 23 27 31 35 57 — 46 71 72 73 83 85 99
TRUE PP3V3_S5_AVREF_SMC 45 46
TRUE PP3V42_G3H 53 64 65 66 — 6 7 21 23 43 45 46 47 48 49 53 64 65 73
TRUE PP5V_S0 6 7 23 42 47 52 54 68 69 70 72 86 88
TRUE PP5V_S3 7 31 33 42 43 44 46 54 56 58 61 66 67 72 82 101
TRUE PP5V_S5 7 23 66 72
TRUE PPBUS_G3H 7 40 49 65 66 67 69 70 82 86 89
TRUE PPDCIN_G3H 7 64 65
TRUE PPVCORE_GPU 7 49 75 82
TRUE PPVCORE_S0_CPU 7 12 15 49 68
TRUE PPVCORE_S0_GFX 7 13 24 49 69
TRUE PPVP_FW 7 40 41
TRUE PPVTTDDR_S3 7 32 67

FUNC_TEST

TRUE BKLT_EN 88
TRUE TP_ISSP_SCLK_P1_1 8 53
TRUE TP_ISSP_SDATA_P1_0 8 53
TRUE LCD_BKLT_PWM 87 88
TRUE LPCPLUS_GPIO 20 47
TRUE LPCPLUS_RESET_L 27 47 87 94
TRUE LPC_AD<0..3> 17 45 47 87 94
TRUE LPC_CLK33M_LPCPLUS 27 47 94
TRUE LPC_FRAME_L 17 45 47 87 94
TRUE LPC_PWRDWN_L 18 45 47
TRUE LPC_SERIRQ 17 45 47
TRUE PM_CLKRUN_L 18 45 47
TRUE PM_SYSRST_L 18 27 45
TRUE SMC_MD1 45 47
TRUE SMC_NMI 45 47
TRUE SMC_ONOFF_L 45 46 53
TRUE SMC_RESET_L 45 46 47 65
TRUE SMC_RX_L 43 45 46 47
TRUE SMC_TCK 45 46 47
TRUE SMC_TDI 45 46 47
TRUE SMC_TDO 45 46 47
TRUE SMC_TMS 45 46 47
TRUE SMC_TRST_L 45 47
TRUE SMC_TX_L 43 45 46 47
TRUE SPIROM_USE_MLB 20 47 57
TRUE SPI_ALT_CLK 47
TRUE SPI_ALT_CS_L 47
TRUE SPI_ALT_MISO 47
TRUE SPI_ALT_MOSI 47
TRUE SYS_LED_ANODE_R 42

ICT Test Points

CPU NO_TESTs

NO_TEST
TP_CPU_RSVD<65..62> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<65..62>
TP_CPU_RSVD<58..45> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<58..45>
TP_CPU_RSVD<43..32> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<43..32>
TP_CPU_RSVD<27..26> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<27..26>
TP_CPU_RSVD<24..15> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<24..15>
TP_CPU_RSVD<2..1> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD<2..1>
TP_CPU_RSVD_NCTF<8..5> — TRUE — MAKE_BASE=TRUE — NC_TP_CPU_RSVD_NCTF<8..5>

NC NO_TESTs

NO_TEST
NC_CRT_IG_BLUE — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_BLUE
NC_CRT_IG_GREEN — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_GREEN
NC_CRT_IG_RED — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_RED
NC_CRT_IG_DDC_CLK — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_DDC_CLK
NC_CRT_IG_DDC_DATA — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_DDC_DATA
NC_CRT_IG_HSYNC — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_HSYNC
NC_CRT_IG_VSYNC — TRUE — MAKE_BASE=TRUE — NC_CRT_IG_VSYNC
NC_LVDS_IG_CTRL_CLK — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_CTRL_CLK
NC_LVDS_IG_CTRL_DATA — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_CTRL_DATA
NC_PCH_LVDS_VBG — TRUE — MAKE_BASE=TRUE — NC_PCH_LVDS_VBG
NC_HDA_SDIN1 — TRUE — MAKE_BASE=TRUE — NC_HDA_SDIN1
NC_HDA_SDIN2 — TRUE — MAKE_BASE=TRUE — NC_HDA_SDIN2
NC_HDA_SDIN3 — TRUE — MAKE_BASE=TRUE — NC_HDA_SDIN3

NC NO_TESTs

NO_TEST
TP_PCI_AD<31..0> — TRUE — MAKE_BASE=TRUE — NC_PCI_AD<31..0>
TP_PCI_C_BE_L<3..0> — TRUE — MAKE_BASE=TRUE — NC_PCI_C_BE_L<3..0>
NC_PCI_GNT3_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT3_L
NC_PCI_GNT2_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT2_L
NC_PCI_GNT1_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT1_L
NC_PCI_GNT0_L — TRUE — MAKE_BASE=TRUE — NC_PCI_GNT0_L
NC_PCI_PAR — TRUE — MAKE_BASE=TRUE — NC_PCI_PAR
NC_PCI_RESET_L — TRUE — MAKE_BASE=TRUE — NC_PCI_RESET_L
NC_PCI_PME_L — TRUE — MAKE_BASE=TRUE — NC_PCI_PME_L
NC_PCI_CLK33M_OUT3 — TRUE — MAKE_BASE=TRUE — NC_PCI_CLK33M_OUT3
NC_PCH_NV_RCOMP — TRUE — MAKE_BASE=TRUE — NC_PCH_NV_RCOMP
TP_NV_DQ<15..0> — TRUE — MAKE_BASE=TRUE — NC_NV_DQ<15..0>
TP_NV_DQS<1..0> — TRUE — MAKE_BASE=TRUE — NC_NV_DQS<1..0>
TP_NV_CE_L<3..0> — TRUE — MAKE_BASE=TRUE — NC_NV_CE_L<3..0>
NC_NV_ALE — TRUE — MAKE_BASE=TRUE — NC_NV_ALE
NC_NV_CLE — TRUE — MAKE_BASE=TRUE — NC_NV_CLE
NC_NV_RB_L — TRUE — MAKE_BASE=TRUE — NC_NV_RB_L
TP_NV_WR_RE_L<1..0> — TRUE — MAKE_BASE=TRUE — NC_NV_WR_RE_L<1..0>
TP_NV_WE_CK_L<1..0> — TRUE — MAKE_BASE=TRUE — NC_NV_WE_CK_L<1..0>
NC_PCIE_CLK100M_PE4N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE4N
NC_PCIE_CLK100M_PE4P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE4P
NC_PCIE_CLK100M_PE5N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_PE6N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE6N
NC_PCIE_CLK100M_PE6P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE6P
NC_PCIE_CLK100M_PE7N — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE7N
NC_PCIE_CLK100M_PE7P — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE7P
NC_PSOC_P1_3 — TRUE — MAKE_BASE=TRUE — NC_PSOC_P1_3
NC_SATA_C_D2RN — TRUE — MAKE_BASE=TRUE — NC_SATA_C_D2RN
NC_SATA_C_D2RP — TRUE — MAKE_BASE=TRUE — NC_SATA_C_D2RP
NC_SATA_C_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_SATA_C_R2D_CN
NC_SATA_C_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_SATA_C_R2D_CP
NC_SATA_D_D2RN — TRUE — MAKE_BASE=TRUE — NC_SATA_D_D2RN
NC_SATA_D_D2RP — TRUE — MAKE_BASE=TRUE — NC_SATA_D_D2RP
NC_SATA_D_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_SATA_D_R2D_CP
NC_SATA_SSD2_D2RN — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_D2RN
NC_SATA_SSD2_D2RP — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_D2RP
NC_SATA_SSD2_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_R2D_CN
NC_SATA_SSD2_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_SATA_SSD2_R2D_CP
TP_SMC_P41 — TRUE — MAKE_BASE=TRUE — NC_SMC_P41

NC NO_TESTs

NO_TEST
NC_PCIE_PE5_D2RN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE5_D2RN
NC_PCIE_PE5_D2RP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE5_D2RP
NC_PCIE_PE5_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE5_R2D_CN
NC_PCIE_PE5_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE5_R2D_CP
NC_PCIE_PE6_D2RN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE6_D2RN
NC_PCIE_PE6_D2RP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE6_D2RP
NC_PCIE_PE6_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE6_R2D_CN
NC_PCIE_PE6_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE6_R2D_CP
NC_PCIE_PE7_D2RN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE7_D2RN
NC_PCIE_PE7_D2RP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE7_D2RP
NC_PCIE_PE7_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE7_R2D_CN
NC_PCIE_PE7_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE7_R2D_CP
NC_PCIE_PE8_D2RN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE8_D2RN
NC_PCIE_PE8_D2RP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE8_D2RP
NC_PCIE_PE8_R2D_CN — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE8_R2D_CN
NC_PCIE_PE8_R2D_CP — TRUE — MAKE_BASE=TRUE — NC_PCIE_PE8_R2D_CP
NC_CLINK_CLK — TRUE — MAKE_BASE=TRUE — NC_CLINK_CLK
NC_CLINK_DATA — TRUE — MAKE_BASE=TRUE — NC_CLINK_DATA
NC_CLINK_RESET_L — TRUE — MAKE_BASE=TRUE — NC_CLINK_RESET_L
NC_PCIE_CLK100M_PEBN — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PEBN
NC_PCIE_CLK100M_PEBP — TRUE — MAKE_BASE=TRUE — NC_PCIE_CLK100M_PEBP

NC NO_TESTs

NO_TEST
NC_SMC_FAN_3_TACH 45 46
NC_SMC_FAN_3_CTL 45 46
NC_SMC_FAN_2_TACH 45 46
NC_SMC_FAN_2_CTL 45 46
NC_FW2_TPBP 39 41
NC_FW2_TPBN 39 41
NC_FW2_TPBIAS 39 41
NC_FW2_TPAP 39 41
NC_FW2_TPAN 39 41
NC_FW0_TPBP 39 41 96
NC_FW0_TPBN 39 41 96
NC_FW0_TPAP 39 41 96
NC_ESTARLDO_EN 45 46
NC_ALS_GAIN 45 46
NC_FW643_AVREG — TRUE — MAKE_BASE=TRUE — NC_FW643_AVREG
NC_FW643_TDI — TRUE — MAKE_BASE=TRUE — NC_FW643_TDI
NC_DP_IG_C_HPD — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_HPD
NC_DP_IG_C_CTRL_CLK — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_CTRL_CLK
NC_DP_IG_C_CTRL_DATA — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_CTRL_DATA
TP_DP_IG_C_MLP<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_MLP<3..0>
TP_DP_IG_C_MLN<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_MLN<3..0>
NC_DP_IG_C_AUXP — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_AUXP
NC_DP_IG_C_AUXN — TRUE — MAKE_BASE=TRUE — NC_DP_IG_C_AUXN
NC_DP_IG_D_HPD — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_HPD
NC_DP_IG_D_CTRL_CLK — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_CTRL_CLK
NC_DP_IG_D_CTRL_DATA — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_CTRL_DATA
TP_DP_IG_D_MLP<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_MLP<3..0>
TP_DP_IG_D_MLN<3..0> — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_MLN<3..0>
NC_DP_IG_D_AUXP — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_AUXP
NC_DP_IG_D_AUXN — TRUE — MAKE_BASE=TRUE — NC_DP_IG_D_AUXN
NC_SDVO_TVCLKINN — TRUE — MAKE_BASE=TRUE — NC_SDVO_TVCLKINN
NC_SDVO_TVCLKINP — TRUE — MAKE_BASE=TRUE — NC_SDVO_TVCLKINP
NC_SDVO_STALLN — TRUE — MAKE_BASE=TRUE — NC_SDVO_STALLN
NC_SDVO_STALLP — TRUE — MAKE_BASE=TRUE — NC_SDVO_STALLP
NC_SDVO_INTN — TRUE — MAKE_BASE=TRUE — NC_SDVO_INTN
NC_SDVO_INTP — TRUE — MAKE_BASE=TRUE — NC_SDVO_INTP
NC_GPU_BUFRST_L — TRUE — MAKE_BASE=TRUE — NC_GPU_BUFRST_L 6 74
TP_GPU_GSTATE<0> — TRUE — MAKE_BASE=TRUE — NC_GPU_GSTATE<0>
TP_GPU_GSTATE<1> — TRUE — MAKE_BASE=TRUE — NC_GPU_GSTATE<1>
TP_GPU_MIOA_D<9..0> — TRUE — MAKE_BASE=TRUE — NC_GPU_MIOA_D<9..0>
TP_GPU_MIOA_DE — TRUE — MAKE_BASE=TRUE — NC_GPU_MIOA_DE
NC_LVDS_EG_BKL_PWM — TRUE — MAKE_BASE=TRUE — NC_LVDS_EG_BKL_PWM
TP_LVDS_IG_B_CLKN — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_B_CLKN
TP_LVDS_IG_B_CLKP — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_B_CLKP
TP_LVDS_IG_BKL_PWM — TRUE — MAKE_BASE=TRUE — NC_LVDS_IG_BKL_PWM
NC_SMC_BS_ALRT_L — TRUE — MAKE_BASE=TRUE — NC_SMC_BS_ALRT_L
NC_PCH_SST — TRUE — MAKE_BASE=TRUE — NC_PCH_SST
NC_PCH_NC1 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC1
NC_PCH_NC2 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC2
NC_PCH_NC3 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC3
NC_PCH_NC4 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC4
NC_PCH_NC5 — TRUE — MAKE_BASE=TRUE — NC_PCH_NC5
NC_PCH_TP19 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP19
NC_PCH_TP18 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP18
NC_PCH_TP17 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP17
NC_PCH_TP16 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP16
NC_PCH_TP15 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP15
NC_PCH_TP14 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP14
NC_PCH_TP13 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP13
NC_PCH_TP12 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP12
NC_PCH_TP11 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP11
NC_PCH_TP10 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP10
NC_PCH_TP9 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP9
NC_PCH_TP8 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP8
NC_PCH_TP7 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP7
NC_PCH_TP6 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP6
NC_PCH_TP5 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP5
NC_PCH_TP4 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP4
NC_PCH_TP3 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP3
NC_PCH_TP2 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP2
NC_PCH_TP1 — TRUE — MAKE_BASE=TRUE — NC_PCH_TP1
PCH_VSS_NCTF<1> 20 94
PCH_VSS_NCTF<2> 20 94
PCH_VSS_NCTF<5> 20 94
PCH_VSS_NCTF<7>
PCH_VSS_NCTF<9> 20 94
PCH_VSS_NCTF<11> 20 94
PCH_VSS_NCTF<12> 20 94
PCH_VSS_NCTF<15> 20 94
PCH_VSS_NCTF<17> 20 94
PCH_VSS_NCTF<19> 6 20 94
PCH_VSS_NCTF<19> 6 20 94
PCH_VSS_NCTF<21> 20 94
PCH_VSS_NCTF<25> 20 94
PCH_VSS_NCTF<27> 20 94
PCH_VSS_NCTF<29> 20 94

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PAGE TITLE
Functional / ICT Test

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 7 OF 132
SHEET 6 OF 101

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"G3Hot" (Always-Present) Rails

- PPBUS_G3H — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
  - PPBUS_G3H
- PPBUS_CPU_IMVP_ISNS — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V, MAKE_BASE=TRUE
  - PPBUS_CPU_IMVP_ISNS
- PPDCIN_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=18.5V, MAKE_BASE=TRUE
  - PPDCIN_G3H
- PP3V42_G3H — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
  - PP3V42_G3H
  - PP3V42_G3H
  - PP3V42_G3H
  - PP3V42_G3H
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  - PP3V42_G3H
  - PP3V42_G3H
  - PP3V42_G3H
  - PP3V42_G3H

5V Rails

- PP5V_S5 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE
  - PP5V_S5
  - PP5V_S5
  - PP5V_S5
- PP5V_S3 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
  - PP5V_S3
- PP5V_S0 — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0
  - PP5V_S0

3.3V Rails

- PP3V3_S5 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
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  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
  - PP3V3_S5
- PP3V3_S3 — MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
  - PP3V3_S3
- PP3V3_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
  - PP3V3_S0
  - PP3V3_S0
  - PP3V3_S0

Thermal Module Holes

ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0940 3R2P5 — GND
ZT0950 TH — GND
SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND
ZT0990 3R2P5 — GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0904 2.0DIA-TALL-EMI-MLB-M97-M98

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0901 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0917 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
GND_CHASSIS_AUDIO_JACK 42

GMUX ALIASES

87 86 82 73 8	PM_ALL_GPU_PGOOD (MAKE_BASE=TRUE)	PM_ALL_GPU_PGOOD	8 73 82 86 87
87 8	TP_LVDS_MUX_SEL_EG (MAKE_BASE=TRUE)	TP_LVDS_MUX_SEL_EG	8 87
87 74 8	EG_RESET_L (MAKE_BASE=TRUE)	EG_RESET_L	8 74 87
87 18 8	LVDS_IG_BKL_ON (MAKE_BASE=TRUE)	LVDS_IG_BKL_ON	8 18 87
87 18 8	LVDS_IG_PANEL_PWR (MAKE_BASE=TRUE)	LVDS_IG_PANEL_PWR	8 18 87
89 87 8	LCD_BKLT_EN (MAKE_BASE=TRUE)	LCD_BKLT_EN	8 87 89
87 74 8	PEX_CLKREQ_L (MAKE_BASE=TRUE)	PEX_CLKREQ_L	8 74 87
87 17 8	PEG_CLKREQ_L (MAKE_BASE=TRUE)	PEG_CLKREQ_L	8 17 87
73 71 8	PM_ENET_EN (MAKE_BASE=TRUE)	PM_ENET_EN	8 71 73
40 20 8	FW_PLUG_DET_L (MAKE_BASE=TRUE)	FW_PLUG_DET_L	8 20 40
40 39 8	FW643_WAKE_L (MAKE_BASE=TRUE)	FW643_WAKE_L	8 39 40
45 8	TP_SMC_EXCARD_PWR_EN (MAKE_BASE=TRUE)	TP_SMC_EXCARD_PWR_EN	8 45
17 8	NC_SATA_EXTA_D2R_N (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_SATA_EXTA_D2R_N	8 17
17 8	NC_SATA_EXTA_D2R_P (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_SATA_EXTA_D2R_P	8 17
17 8	NC_SATA_EXTA_R2D_C_N (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_SATA_EXTA_R2D_C_N	8 17
17 8	NC_SATA_EXTA_R2D_C_P (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_SATA_EXTA_R2D_C_P	8 17
17 8	NC_PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_PCIE_EXCARD_D2R_N	8 17
17 8	NC_PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_PCIE_EXCARD_D2R_P	8 17
17 8	NC_PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_PCIE_EXCARD_R2D_C_N	8 17
17 8	NC_PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_PCIE_EXCARD_R2D_C_P	8 17
94 17 8	NC_PCIE_CLK100M_EXCARD_N (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_PCIE_CLK100M_EXCARD_N	8 17 94
94 17 8	NC_PCIE_CLK100M_EXCARD_P (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_PCIE_CLK100M_EXCARD_P	8 17 94
53 8 6	TP_ISSP_SCLK_P1_1 (MAKE_BASE=TRUE)	TP_ISSP_SCLK_P1_1	6 8 53
53 8 6	TP_ISSP_SDATA_P1_0 (MAKE_BASE=TRUE)	TP_ISSP_SDATA_P1_0	6 8 53

GND
GND
GND
GND
GND

CPU signals

91 15 12	CPU_VID<0..6> (MAKE_BASE=TRUE)	CPUIMVP_VID<0..6>	68
91 13	GFX_VID<0..6> (MAKE_BASE=TRUE)	GFXIMVP_VID<0..6>	69
67 31 8	MEMVTT_EN (MAKE_BASE=TRUE)	MEMVTT_EN	8 31 67
91 12 8	TP_CPU_VTT_SELECT (MAKE_BASE=TRUE)	TP_CPU_VTT_SELECT	8 12 91

GPU signals

91 74 9	PEG_D2R_P<15..0> (MAKE_BASE=TRUE)	=PEG_D2R_P<0..15>	
91 74	PEG_D2R_N<15..0> (MAKE_BASE=TRUE)	=PEG_D2R_N<0..15>	9
91 74 9	PEG_R2D_C_P<15..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<0..15>	
91 74	PEG_R2D_C_N<15..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<0..15>	9

** PEG LANES REVERSED. ARD STRAP REQ'D. **

R0902 3.0K 5% 1/16W MF-LF 402
91 25 5 CPU_CFG<3> — 1 — 2

93 18 8 6	TP_LVDS_IG_B_CLKP (MAKE_BASE=TRUE)	TP_LVDS_IG_B_CLKP	6 8 18 93
93 18 8 6	TP_LVDS_IG_B_CLKN (MAKE_BASE=TRUE)	TP_LVDS_IG_B_CLKN	6 8 18 93
18 8 6	TP_LVDS_IG_BKL_PWM (MAKE_BASE=TRUE)	TP_LVDS_IG_BKL_PWM	6 8 18
74 5	NC_GPU_XTALOUT (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_GPU_XTALOUT	8 79
93 18 8	NC_LVDS_IG_A_DATAP<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_A_DATAP<3>	8 18 93
93 18 8	NC_LVDS_IG_A_DATAN<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_A_DATAN<3>	8 18 93
93 84	DP_IG_ML_P<3..0> (MAKE_BASE=TRUE)	DP_IG_B_ML_P<3..0>	18
93 84	DP_IG_ML_N<3..0> (MAKE_BASE=TRUE)	DP_IG_B_ML_N<3..0>	18
93 18 8	NC_LVDS_IG_B_DATAP<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_B_DATAP<3>	8 18 93
93 18 8	NC_LVDS_IG_B_DATAN<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_B_DATAN<3>	8 18 93
93 84 18 8	DP_IG_AUX_CH_P (MAKE_BASE=TRUE)	DP_IG_AUX_CH_P	8 18 84 93
93 84 18 8	DP_IG_AUX_CH_N (MAKE_BASE=TRUE)	DP_IG_AUX_CH_N	8 18 84 93
84 80 18 8	DP_IG_DDC_CLK (MAKE_BASE=TRUE)	DP_IG_DDC_CLK	8 18 80 84
84 80 18 8	DP_IG_DDC_DATA (MAKE_BASE=TRUE)	DP_IG_DDC_DATA	8 18 80 84
84 18 8	DP_IG_HPD (MAKE_BASE=TRUE)	DP_IG_HPD	8 18 84
35 8	NC_USB_HUB1_OCS4 (MAKE_BASE=TRUE)	NC_USB_HUB1_OCS4	8 35
36 8	NC_USB_HUB2_OCS3 (MAKE_BASE=TRUE)	NC_USB_HUB2_OCS3	8 36
93 36 34 8	USB_SDCARD_P (MAKE_BASE=TRUE)	USB_SDCARD_P	8 34 36 93
93 36 34 8	USB_SDCARD_N (MAKE_BASE=TRUE)	USB_SDCARD_N	8 34 36 93

54 53 50 48 36 35 34 33 32 31 20 17 7 6 101 87 73 72 55 PP3V3_S3

R0903 10K 5% 1/16W MF-LF 402 — 1 — 2
R0904 10K 5% 1/16W MF-LF 402 — 1 — 2
USB_EXTC_N 35 93
USB_EXTC_P 35 93

78 77 76 75 56 50 7 6 PP1V8R1V55_S0GPU_ISNS

R0900 10 1% 1/16W MF-LF 402 — 1 — 2
GPU_FB_A_VREF_DIV 8 32 77 (MAKE_BASE=TRUE)
GPU_FB_A_VREF_DIV 8 32 77

R0901 10 1% 1/16W MF-LF 402 — 1 — 2
GPU_FB_B_VREF_DIV 8 32 78 (MAKE_BASE=TRUE)
GPU_FB_B_VREF_DIV 8 32 78

Digital Ground

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V

SYNC_MASTER=K17_REF SYNC_DATE=06/11/2009

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 9 OF 132
SHEET: 8 OF 101

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U1000
ARRANDALE
BGA
(SYM 1 OF 11)

DMI

DMI_S2N_N<0>	F7	DMI_RX0*
DMI_S2N_N<1>	J8	DMI_RX1*
DMI_S2N_N<2>	K8	DMI_RX2*
DMI_S2N_N<3>	J4	DMI_RX3*
DMI_S2N_P<0>	F9	DMI_RX0
DMI_S2N_P<1>	J6	DMI_RX1
DMI_S2N_P<2>	K9	DMI_RX2
DMI_S2N_P<3>	J2	DMI_RX3
DMI_N2S_N<0>	H17	DMI_TX0*
DMI_N2S_N<1>	K15	DMI_TX1*
DMI_N2S_N<2>	J13	DMI_TX2*
DMI_N2S_N<3>	F10	DMI_TX3*
DMI_N2S_P<0>	G17	DMI_TX0
DMI_N2S_P<1>	M15	DMI_TX1
DMI_N2S_P<2>	G13	DMI_TX2
DMI_N2S_P<3>	J11	DMI_TX3

FLEXIBLE DISPLAY INTERFACE

FDI_DATA_N<0>	L2	FDI_TX0*
FDI_DATA_N<1>	N7	FDI_TX1*
FDI_DATA_N<2>	M4	FDI_TX2*
FDI_DATA_N<3>	P1	FDI_TX3*
FDI_DATA_N<4>	N10	FDI_TX4*
FDI_DATA_N<5>	R7	FDI_TX5*
FDI_DATA_N<6>	U7	FDI_TX6*
FDI_DATA_N<7>	W8	FDI_TX7*
FDI_DATA_P<0>	K1	FDI_TX0
FDI_DATA_P<1>	N5	FDI_TX1
FDI_DATA_P<2>	N2	FDI_TX2
FDI_DATA_P<3>	R2	FDI_TX3
FDI_DATA_P<4>	N9	FDI_TX4
FDI_DATA_P<5>	R8	FDI_TX5
FDI_DATA_P<6>	U6	FDI_TX6
FDI_DATA_P<7>	W10	FDI_TX7
FDI_FSYNC<0>	AC7	FDI_FSYNC0
FDI_FSYNC<1>	AC9	FDI_FSYNC1
FDI_INT	AB5	FDI_INT
FDI_LSYNC<0>	AA1	FDI_LSYNC0
FDI_LSYNC<1>	AB2	FDI_LSYNC1

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI	B12	
PEG_ICOMPO	A13	
PEG_RCOMPO	D12	
PEG_RBIAS	B11	
PEG_RX0*	G40	=PEG_D2R_N<0>
PEG_RX1*	G38	=PEG_D2R_N<1>
PEG_RX2*	H34	=PEG_D2R_N<2>
PEG_RX3*	P34	=PEG_D2R_N<3>
PEG_RX4*	G28	=PEG_D2R_N<4>
PEG_RX5*	H25	=PEG_D2R_N<5>
PEG_RX6*	H24	=PEG_D2R_N<6>
PEG_RX7*	D29	=PEG_D2R_N<7>
PEG_RX8*	B26	=PEG_D2R_N<8>
PEG_RX9*	D26	=PEG_D2R_N<9>
PEG_RX10*	B23	=PEG_D2R_N<10>
PEG_RX11*	D22	=PEG_D2R_N<11>
PEG_RX12*	A20	=PEG_D2R_N<12>
PEG_RX13*	D19	=PEG_D2R_N<13>
PEG_RX14*	A17	=PEG_D2R_N<14>
PEG_RX15*	B14	=PEG_D2R_N<15>
PEG_RX0	F40	PEG_D2R_P<15>
PEG_RX1	J38	PEG_D2R_P<14>
PEG_RX2	G34	PEG_D2R_P<13>
PEG_RX3	M34	PEG_D2R_P<12>
PEG_RX4	J28	PEG_D2R_P<11>
PEG_RX5	G25	PEG_D2R_P<10>
PEG_RX6	K24	PEG_D2R_P<9>
PEG_RX7	B28	PEG_D2R_P<8>
PEG_RX8	A27	PEG_D2R_P<7>
PEG_RX9	B25	PEG_D2R_P<6>
PEG_RX10	A24	PEG_D2R_P<5>
PEG_RX11	B21	PEG_D2R_P<4>
PEG_RX12	B19	PEG_D2R_P<3>
PEG_RX13	B18	PEG_D2R_P<2>
PEG_RX14	B16	PEG_D2R_P<1>
PEG_RX15	D15	PEG_D2R_P<0>
PEG_TX0*	N40	=PEG_R2D_C_N<0>
PEG_TX1*	L38	=PEG_R2D_C_N<1>
PEG_TX2*	M32	=PEG_R2D_C_N<2>
PEG_TX3*	D40	=PEG_R2D_C_N<3>
PEG_TX4*	A38	=PEG_R2D_C_N<4>
PEG_TX5*	G32	=PEG_R2D_C_N<5>
PEG_TX6*	B33	=PEG_R2D_C_N<6>
PEG_TX7*	B35	=PEG_R2D_C_N<7>
PEG_TX8*	L30	=PEG_R2D_C_N<8>
PEG_TX9*	A31	=PEG_R2D_C_N<9>
PEG_TX10*	B32	=PEG_R2D_C_N<10>
PEG_TX11*	L28	=PEG_R2D_C_N<11>
PEG_TX12*	N26	=PEG_R2D_C_N<12>
PEG_TX13*	M24	=PEG_R2D_C_N<13>
PEG_TX14*	G21	=PEG_R2D_C_N<14>
PEG_TX15*	J20	=PEG_R2D_C_N<15>
PEG_TX0	L40	PEG_R2D_C_P<15>
PEG_TX1	N38	PEG_R2D_C_P<14>
PEG_TX2	N32	PEG_R2D_C_P<13>
PEG_TX3	B39	PEG_R2D_C_P<12>
PEG_TX4	B37	PEG_R2D_C_P<11>
PEG_TX5	H32	PEG_R2D_C_P<10>
PEG_TX6	A34	PEG_R2D_C_P<9>
PEG_TX7	D36	PEG_R2D_C_P<8>
PEG_TX8	J30	PEG_R2D_C_P<7>
PEG_TX9	B30	PEG_R2D_C_P<6>
PEG_TX10	D33	PEG_R2D_C_P<5>
PEG_TX11	N28	PEG_R2D_C_P<4>
PEG_TX12	M25	PEG_R2D_C_P<3>
PEG_TX13	N24	PEG_R2D_C_P<2>
PEG_TX14	F21	PEG_R2D_C_P<1>
PEG_TX15	L20	PEG_R2D_C_P<0>

CPU_PEG_COMP

CPU_PEG_RBIAS

R1012 750 1% 1/16W MF-LF 402

R1010 49.9 1% 1/16W MF-LF 402

Embedded DisplayPort (eDP) pins (Auburndale only):

eDP_AUX#

NOTE: HPD must be inverted and level-shifted for Auburndale (1.05V).

eDP_HPD#
eDP_AUX

eDP_TX#<3>
eDP_TX#<2>
eDP_TX#<1>
eDP_TX#<0>

eDP_TX<3>
eDP_TX<2>
eDP_TX<1>
eDP_TX<0>

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(SYM 5 OF 11)

RESERVED

CPU_CFG<0>	AL4	CFG0 (IPU)
CPU_CFG<1>	AM2	CFG1 (IPU)
CPU_CFG<2>	AK1	CFG2 (IPU)
CPU_CFG<3>	AK2	CFG3 (IPU)
CPU_CFG<4>	AK4	CFG4 (IPU)
CPU_CFG<5>	AJ2	CFG5 (IPU)
CPU_CFG<6>	AT2	CFG6 (IPU)
CPU_CFG<7>	AG7	CFG7 (IPU)
CPU_CFG<8>	AF4	CFG8 (IPU)
CPU_CFG<9>	AG2	CFG9 (IPU)
CPU_CFG<10>	AH1	CFG10 (IPU)
CPU_CFG<11>	AC2	CFG11 (IPU)
CPU_CFG<12>	AC4	CFG12 (IPU)
CPU_CFG<13>	AE2	CFG13 (IPU)
CPU_CFG<14>	AD1	CFG14 (IPU)
CPU_CFG<15>	AF8	CFG15 (IPU)
CPU_CFG<16>	AF6	CFG16 (IPU)
CPU_CFG<17>	AB7	CFG17 (IPU)
TP_CPU_RSVD_TP0	AU1	RSVD_TP0
TP_CPU_RSVD<15>	T4	RSVD15
TP_CPU_RSVD<16>	T2	RSVD16
TP_CPU_RSVD<17>	U1	RSVD17
TP_CPU_RSVD<18>	V2	RSVD18
TP_CPU_RSVD<19>	AV71	RSVD19
TP_CPU_RSVD<20>	AW70	RSVD20
TP_CPU_RSVD<21>	AY69	RSVD21
TP_CPU_RSVD<22>	BB69	RSVD22
TP_CPU_RSVD<23>	D8	RSVD23
TP_CPU_RSVD<24>	B7	RSVD24
TP_CPU_RSVD<26>	A10	RSVD26
TP_CPU_RSVD<27>	B9	RSVD27
NC_TP_CPU_RSVD_NCTF<7>	C5	RSVD_NCTF7
NC_TP_CPU_RSVD_NCTF<8>	A6	RSVD_NCTF8
NC_TP_CPU_RSVD_NCTF<6>	E3	RSVD_NCTF6
NC_TP_CPU_RSVD_NCTF<5>	F1	RSVD_NCTF5

RSVD32	W66	NC_TP_CPU_RSVD<32>
RSVD33	W64	NC_TP_CPU_RSVD<33>
RSVD34	AC69	NC_TP_CPU_RSVD<34>
RSVD35	AC71	NC_TP_CPU_RSVD<35>
RSVD36	AA71	NC_TP_CPU_RSVD<36>
RSVD37	AA69	NC_TP_CPU_RSVD<37>
RSVD38	R66	NC_TP_CPU_RSVD<38>
RSVD39	R64	NC_TP_CPU_RSVD<39>
RSVD_NCTF3	BT5	NC_TP_CPU_RSVD<40>
RSVD_NCTF4	BR5	NC_TP_CPU_RSVD<41>
RSVD_NCTF2	BV6	NC_TP_CPU_RSVD<42>
RSVD_NCTF1	BV8	NC_TP_CPU_RSVD<43>
RSVD45	AV69	TP_CPU_RSVD<45>
RSVD46	AK71	TP_CPU_RSVD<46>
RSVD47	AN69	TP_CPU_RSVD<47>
RSVD48	AP66	TP_CPU_RSVD<48>
RSVD49	AH66	TP_CPU_RSVD<49>
RSVD50	AK66	TP_CPU_RSVD<50>
RSVD51	AR71	TP_CPU_RSVD<51>
RSVD52	AM66	TP_CPU_RSVD<52>
RSVD53	AK69	TP_CPU_RSVD<53>
RSVD54	AU71	TP_CPU_RSVD<54>
RSVD55	AT70	TP_CPU_RSVD<55>
RSVD56	AR69	TP_CPU_RSVD<56>
RSVD57	AU69	TP_CPU_RSVD<57>
RSVD58	AT67	TP_CPU_RSVD<58>
RSVD_TP2	AP2	TP_CPU_RSVD<2>
RSVD_TP1	AN7	TP_CPU_RSVD<1>
RSVD62	AV4	CPU_THERMD_P
RSVD63	AU2	CPU_THERMD_N
RSVD64	BE69	TP_CPU_RSVD<64>
RSVD65	BE71	TP_CPU_RSVD<65>
DC_TEST_BV71	BV71	CPU_TEST_BV71_BV69
DC_TEST_BV69	BV69	
DC_TEST_BV68	BV68	TP_CPU_TEST_BV68
DC_TEST_BV5	BV5	TP_CPU_TEST_BV5
DC_TEST_BV3	BV3	CPU_TEST_BV3_BT3
DC_TEST_BV1	BV1	CPU_TEST_BV1_BT1
DC_TEST_BT71	BT71	CPU_TEST_BT71_BT69
DC_TEST_BT69	BT69	
DC_TEST_BT3	BT3	
DC_TEST_BT1	BT1	
DC_TEST_BR71	BR71	TP_CPU_TEST_BR71
DC_TEST_BR1	BR1	TP_CPU_TEST_BR1
DC_TEST_E71	E71	TP_CPU_TEST_E71
DC_TEST_E1	E1	TP_CPU_TEST_E1
DC_TEST_C71	C71	CPU_TEST_C71_A71
DC_TEST_C69	C69	CPU_TEST_C69_A69
DC_TEST_C3	C3	TP_CPU_TEST_C3
DC_TEST_A71	A71	
DC_TEST_A69	A69	
DC_TEST_A68	A68	TP_CPU_TEST_A68
DC_TEST_A5	A5	TP_CPU_TEST_A5

CFG0: PCIe Configuration Select 1 = Single PEG 0 = Bifurcation Enabled
CFG3: PCIe Lane Reversal 1 = Normal Operation 0 = Lanes Reversed
CFG4: Display Port Presence 1 = eDP Disabled 0 = Embedded Display Port Enabled

WF: RSVD nets with arrows have offpage marks on CRB schematic.
WF: RSVD nets with red wires have 0-ohm resistors to GND in CRB schematic.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 10 OF 132
SHEET 9 OF 101

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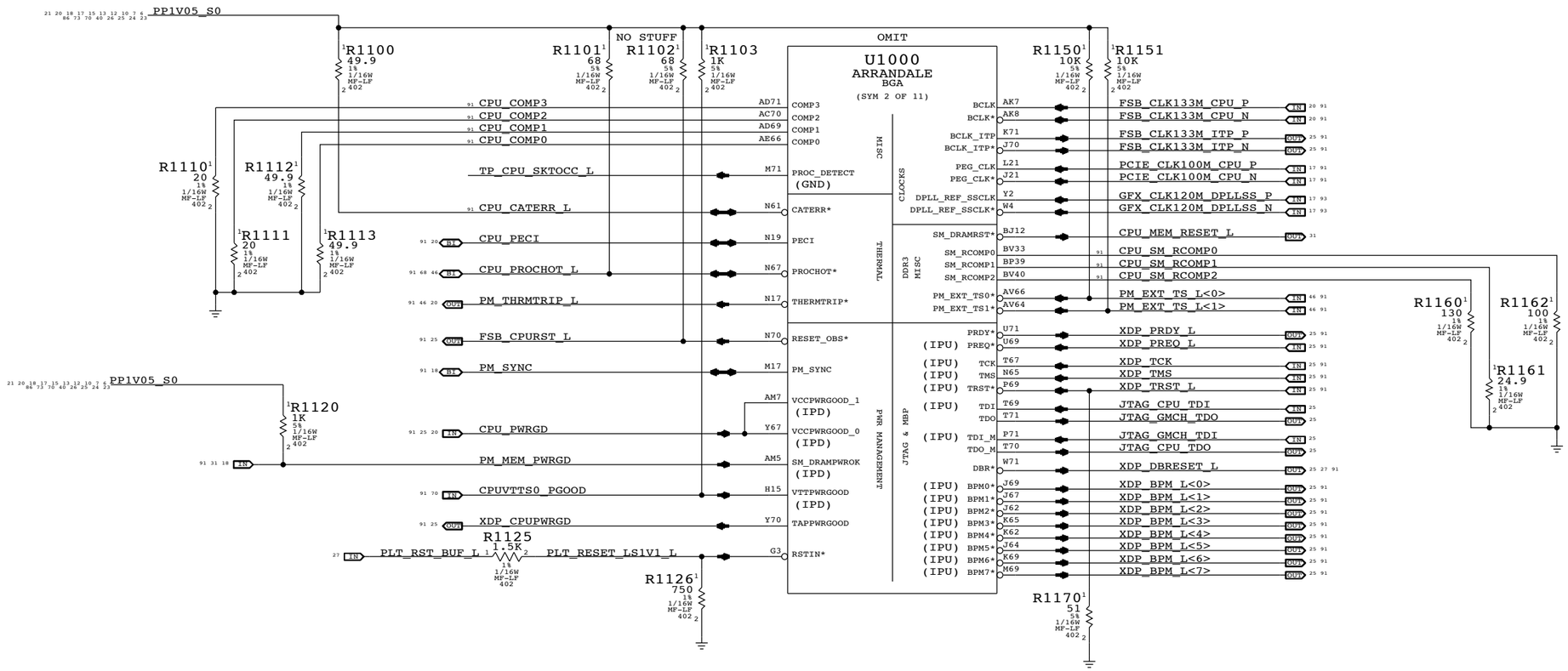

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

CPU Clock/Misc/JTAG

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PAGE 11 OF 132

SHEET 10 OF 101

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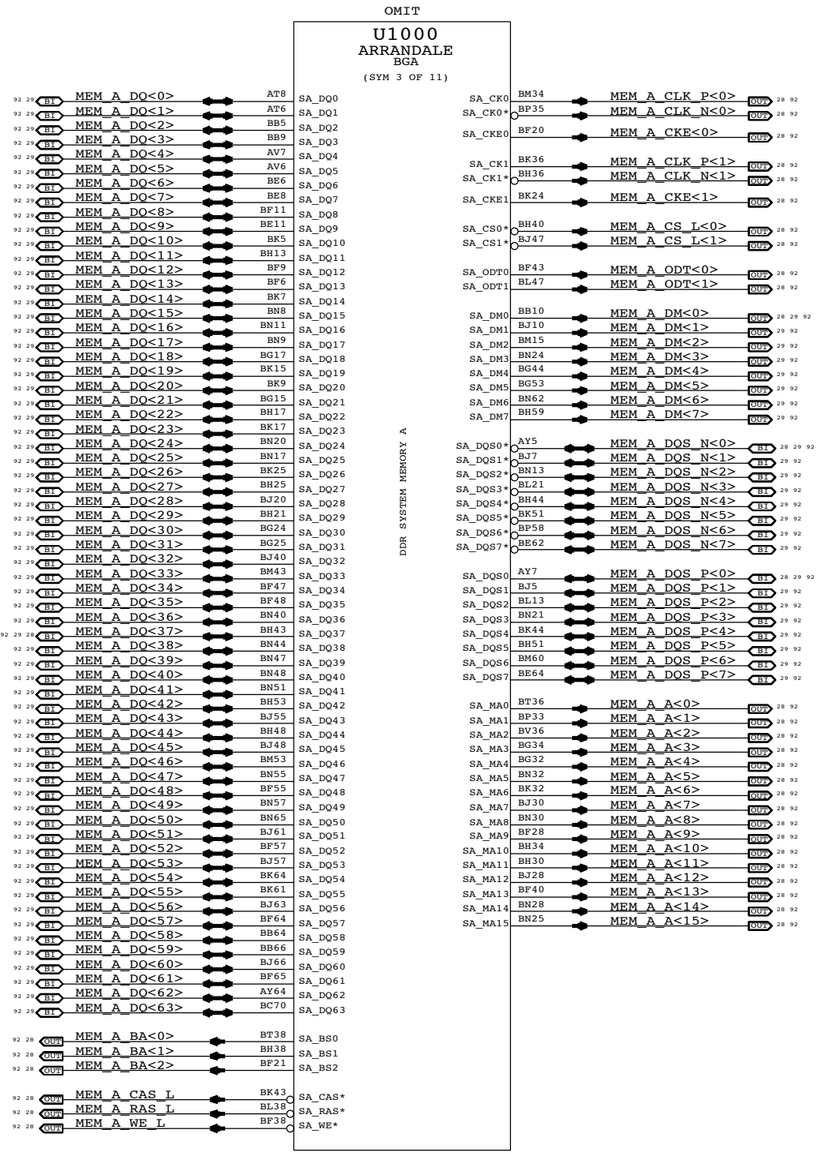

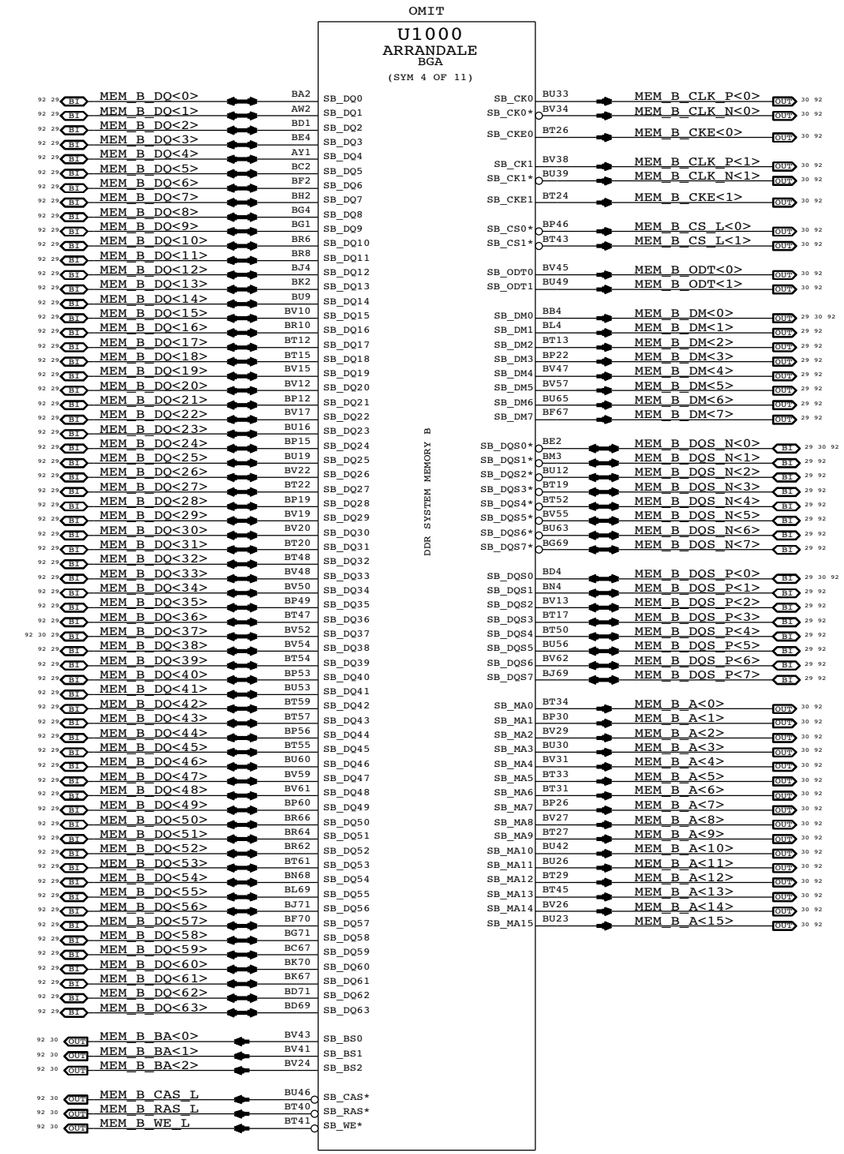

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

CPU DDR3 Interfaces

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PAGE 12 OF 132

SHEET 11 OF 101

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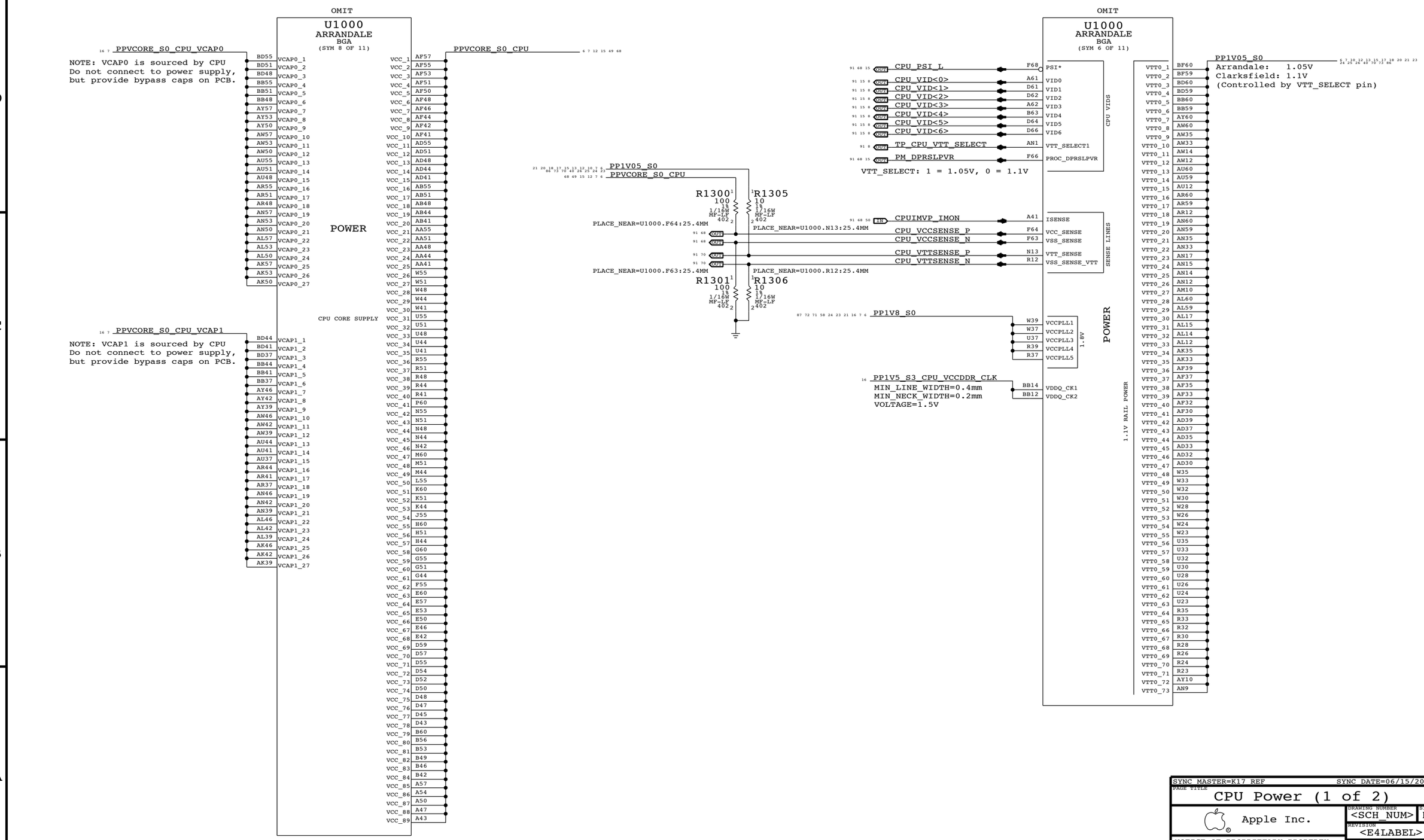

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

CPU Power (1 of 2)

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DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE 13 OF 132

SHEET 12 OF 101

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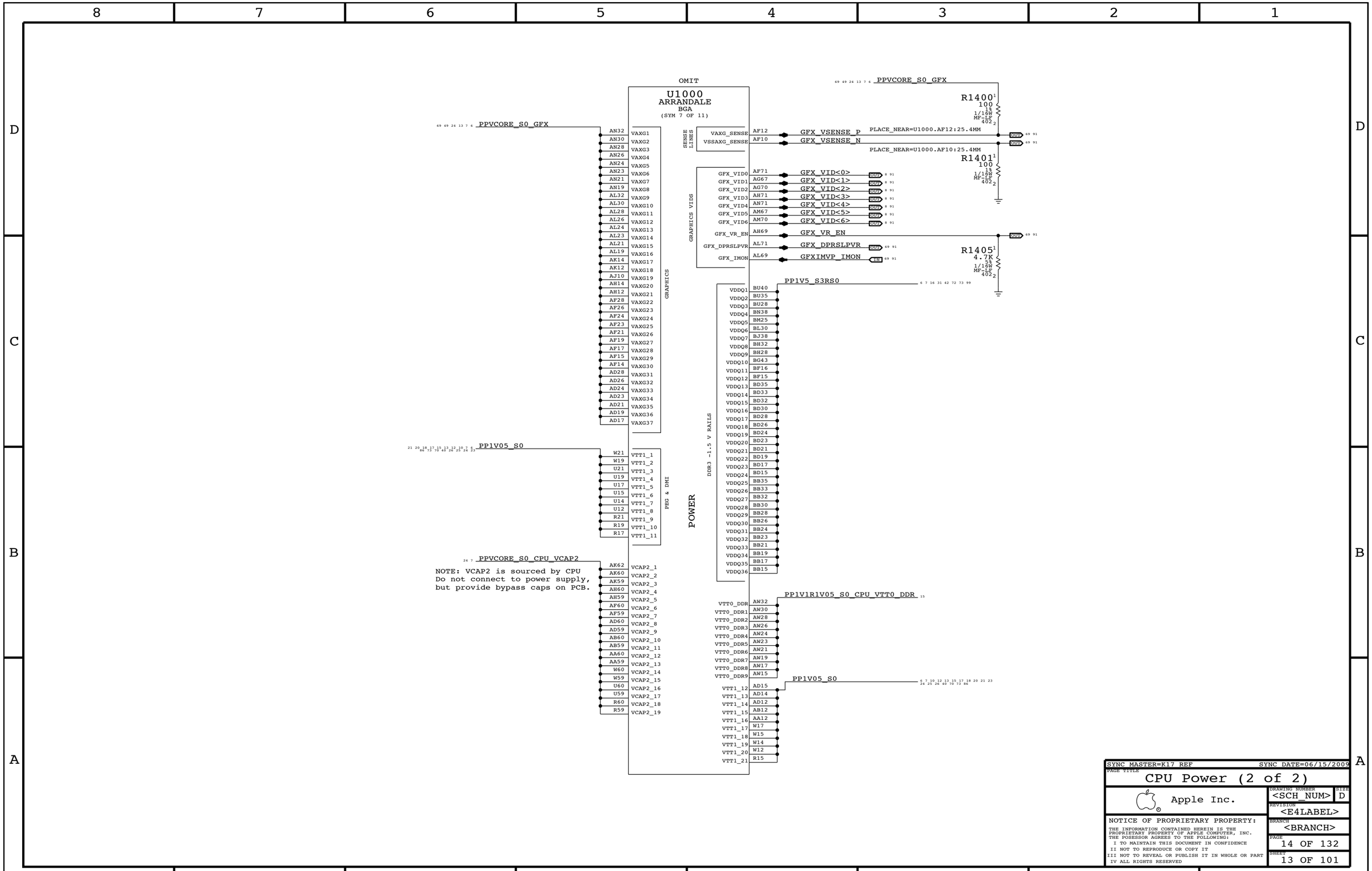

SYNC MASTER=K17 REF	SYNC DATE=06/15/2009
PAGE TITLE	CPU Power (2 of 2)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 14 OF 132
	SHEET 13 OF 101

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U1000 ARRANDALE BGA (SYM 9 OF 11)

BU62	VSS1	VSS76	AY62
BU58	VSS2	VSS77	AY59
BU55	VSS3	VSS78	AY55
BU51	VSS4	VSS79	AY51
BU48	VSS5	VSS80	AY48
BU44	VSS6	VSS81	AY44
BU37	VSS7	VSS82	AY41
BU32	VSS8	VSS83	AY37
BU25	VSS9	VSS84	AY35
BU21	VSS10	VSS85	AY33
BU18	VSS11	VSS86	AY32
BU14	VSS12	VSS87	AY30
BU11	VSS13	VSS88	AY28
BU7	VSS14	VSS89	AY26
BP42	VSS15	VSS90	AY24
BN64	VSS16	VSS91	AY23
BN6	VSS17	VSS92	AY21
BM70	VSS18	VSS93	AY19
BM51	VSS19	VSS94	AY17
BM44	VSS20	VSS95	AY15
BM32	VSS21	VSS96	AY14
BM24	VSS22	VSS97	AY12
BM17	VSS23	VSS98	AY8
BL57	VSS24	VSS99	AY4
BL55	VSS25	VSS100	AW67
BL48	VSS26	VSS101	AW62
BL40	VSS27	VSS102	AW59
BL28	VSS28	VSS103	AW55
BL20	VSS29	VSS104	AW51
BK63	VSS30	VSS105	AW48
BK60	VSS31	VSS106	AW44
BK53	VSS32	VSS107	AW41
BK34	VSS33	VSS108	AW37
BK10	VSS34	VSS109	AV9
BJ64	VSS35	VSS110	AV1
BJ21	VSS36	VSS111	AU70
BJ9	VSS37	VSS112	AU62
BJ1	VSS38	VSS113	AU57
BH70	VSS39	VSS114	AU53
BH57	VSS40	VSS115	AU50
BH55	VSS41	VSS116	AU46
BH47	VSS42	VSS117	AU42
BH24	VSS43	VSS118	AU39
BH20	VSS44	VSS119	AU35
BH15	VSS45	VSS120	AU33
BG51	VSS46	VSS121	AU32
BG36	VSS47	VSS122	AU30
BF62	VSS48	VSS123	AU28
BF30	VSS49	VSS124	AU26
BF13	VSS50	VSS125	AU24
BF8	VSS51	VSS126	AU23
BE70	VSS52	VSS127	AU21
BE65	VSS53	VSS128	AU19
BE9	VSS54	VSS129	AU17
BE1	VSS55	VSS130	AU15
BD57	VSS56	VSS131	AU14
BD53	VSS57	VSS132	AU4
BD50	VSS58	VSS133	AT64
BD46	VSS59	VSS134	AT10
BD42	VSS60	VSS135	AR62
BD39	VSS61	VSS136	AR57
BD14	VSS62	VSS137	AR53
BB71	VSS63	VSS138	AR50
BB62	VSS64	VSS139	AR46
BB57	VSS65	VSS140	AR42
BB53	VSS66	VSS141	AR39
BB50	VSS67	VSS142	AR35
BB46	VSS68	VSS143	AR33
BB42	VSS69	VSS144	AR32
BB39	VSS70	VSS145	AR30
BB7	VSS71	VSS146	AR28
BB1	VSS72	VSS147	AR26
BA70	VSS73	VSS148	AR24
AY71	VSS74	VSS149	AR23
AY66	VSS75	VSS150	AR21

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U1000 ARRANDALE BGA (SYM 10 OF 11)

AR19	VSS151	VSS226	BN71
AR17	VSS152	VSS227	E68
AR15	VSS153	VSS228	AH28
AR14	VSS154	VSS229	AH41
AR4	VSS155	VSS230	A66
AR1	VSS156	VSS231	AH26
AP70	VSS157	VSS232	BN1
AP64	VSS158	VSS233	A64
AN62	VSS159	VSS234	AH24
AN55	VSS160	VSS235	AH39
AN51	VSS161	VSS236	E5
AN48	VSS162	VSS237	AH23
AN44	VSS163	VSS238	C68
AN41	VSS164	VSS239	AH21
AN37	VSS165	VSS240	AH19
AN5	VSS166	VSS241	AH17
AN4	VSS167	VSS242	AH15
AM64	VSS168	VSS243	AH4
AM8	VSS169	VSS244	AG64
AL62	VSS170	VSS245	AG9
AL55	VSS171	VSS246	AG6
AL51	VSS172	VSS247	AF69
AL48	VSS173	VSS248	AF62
AL44	VSS174	VSS249	AF1
AL41	VSS175	VSS250	AE70
AL37	VSS176	VSS251	AE64
AL35	VSS177	VSS252	AD62
AL33	VSS178	VSS253	AD57
AL1	VSS179	VSS254	AD53
AK70	VSS180	VSS255	AD50
AK64	VSS181	VSS256	AD46
AK55	VSS182	VSS257	AD42
AK51	VSS183	VSS258	AD4
AK48	VSS184	VSS259	AC67
AK44	VSS185	VSS260	AC64
AK41	VSS186	VSS261	AC10
AK37	VSS187	VSS262	AC5
AK32	VSS188	VSS263	AC1
AK30	VSS189	VSS264	AB70
AK28	VSS190	VSS265	AB62
AK26	VSS191	VSS266	AB57
AK24	VSS192	VSS267	AB53
AK23	VSS193	VSS268	AB50
AK21	VSS194	VSS269	AB46
AK19	VSS195	VSS270	AB42
AK17	VSS196	VSS271	AB39
AK15	VSS197	VSS272	AB37
AJ70	VSS198	VSS273	AB35
AH62	VSS199	VSS274	AB33
AH57	VSS200	VSS275	AB32
AH55	VSS201	VSS276	AB30
AH53	VSS202	VSS277	AB28
BV66	VSS203	VSS278	AB26
AH51	VSS204	VSS279	AB24
BV64	VSS205	VSS280	AB23
AH50	VSS206	VSS281	AB21
BT68	VSS207	VSS282	AB19
AH48	VSS208	VSS283	AB17
BR69	VSS209	VSS284	AB15
BL71	VSS210	VSS285	AB14
AH46	VSS211	VSS286	AB9
BL1	VSS212	VSS287	AA66
AH37	VSS213	VSS288	AA64
BR68	VSS214	VSS289	AA62
R14	VSS215	VSS290	AA57
AH35	VSS216	VSS291	AA53
AH44	VSS217	VSS292	AA50
H71	VSS218	VSS293	AA46
AH33	VSS219	VSS294	AA42
BR3	VSS220	VSS295	AA39
F71	VSS221	VSS296	AA37
AH32	VSS222	VSS297	AA35
AH42	VSS223	VSS298	AA33
E69	VSS224	VSS299	AA32
AH30	VSS225	VSS300	AA30

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U1000 ARRANDALE BGA (SYM 11 OF 11)

AA28	VSS301	VSS367	K6
AA26	VSS302	VSS368	K4
AA24	VSS303	VSS369	J65
AA23	VSS304	VSS370	J57
AA21	VSS305	VSS371	J48
AA19	VSS306	VSS372	J47
AA17	VSS307	VSS373	J40
AA15	VSS308	VSS374	J9
AA14	VSS309	VSS375	H53
AA4	VSS310	VSS376	H43
W69	VSS311	VSS377	H36
W62	VSS312	VSS378	H1
W57	VSS313	VSS379	G70
W53	VSS314	VSS380	G57
W50	VSS315	VSS381	G53
W46	VSS316	VSS382	G48
W42	VSS317	VSS383	G47
W6	VSS318	VSS384	G43
W1	VSS319	VSS385	G30
V70	VSS320	VSS386	G24
U64	VSS321	VSS387	G20
U62	VSS322	VSS388	G15
U57	VSS323	VSS389	F61
U53	VSS324	VSS390	F48
U50	VSS325	VSS391	F47
U46	VSS326	VSS392	F28
U42	VSS327	VSS393	F20
U39	VSS328	VSS394	F4
U9	VSS329	VSS395	E37
U4	VSS330	VSS396	E33
T1	VSS331	VSS397	E30
R70	VSS332	VSS398	E16
R62	VSS333	VSS399	E12
R57	VSS334	VSS400	D41
R53	VSS335	VSS401	D38
R50	VSS336	VSS402	D34
R46	VSS337	VSS403	D31
R42	VSS338	VSS404	D27
R5	VSS339	VSS405	D24
P4	VSS340	VSS406	D20
N63	VSS341	VSS407	D17
N57	VSS342	VSS408	D13
N53	VSS343	VSS409	D10
N50	VSS344	VSS410	D6
N46	VSS345	VSS411	B65
N30	VSS346	VSS412	B62
N21	VSS347	VSS413	B58
N15	VSS348	VSS414	B55
M53	VSS349	VSS415	B51
M42	VSS350	VSS416	B48
M36	VSS351	VSS417	B44
M1	VSS352	VSS418	A59
L70	VSS353	VSS419	A55
L57	VSS354	VSS420	A52
L48	VSS355	VSS421	A48
L47	VSS356	VSS422	A45
L13	VSS357	VSS423	A40
K64	VSS358	VSS424	A36
K53	VSS359	VSS425	A33
K43	VSS360	VSS426	A29
K36	VSS361	VSS427	A26
K34	VSS362	VSS428	A22
K32	VSS363	VSS429	A19
K25	VSS364	VSS430	A15
K17	VSS365	VSS431	A12
K11	VSS366	VSS432	A8
		VSS433	B40

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
CPU Grounds

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PAGE 15 OF 132

SHEET 14 OF 101

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CPU VCore HF and Bulk Decoupling

4x 470uF 4.5mOhm, 3x 62uF B2, 10x 22uF 0603, 25x 1uF 0402

68 49 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612
1UF 10% 16V X5R 402

C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
1UF 10% 16V X5R 402

PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.

NO STUFF C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1634 C1691 C1692 C1693 C1694 C1698
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

NO STUFF C1635 C1636 C1637 C1638 C1640 C1641 C1642 C1643 C1644 C1645 C1646 C1648
22UF 20% 6.3V X5R-CERM 603

C1649 C1650 C1651 C1652
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NO STUFF C16A0 C16A1 C16A2 C16A3 C16A4
62UF 20% 11V ELEC CASE-B2

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

21 20 18 17 15 13 12 10 7 6 86 73 70 40 26 25 24 23 PP1V05_S0

R1600 1K 5% 1/16W MF-LF 402

R1601 1K 5% 1/16W MF-LF 402

CPUPOC4U R1604 1K 5% 1/16W MF-LF 402

CPUPOC3U R1603 1K 5% 1/16W MF-LF 402

NO STUFF R1606 1K 5% 1/16W MF-LF 402

CPUPOC5U R1605 1K 5% 1/16W MF-LF 402

NO STUFF R1608 1K 5% 1/16W MF-LF 402

R1607 1K 5% 1/16W MF-LF 402

91 12 8 OUT CPU_VID<0>
91 12 8 OUT CPU_VID<1>
91 12 8 OUT CPU_VID<2>
91 12 8 OUT CPU_VID<3>
91 12 8 OUT CPU_VID<4>
91 12 8 OUT CPU_VID<5>
91 12 8 OUT CPU_VID<6>
91 68 12 OUT PM_DPRSLPVR
91 68 12 OUT CPU_PSI_L

NO STUFF R1610 1K 5% 1/16W MF-LF 402

NO STUFF R1612 1K 5% 1/16W MF-LF 402

CPUPOC4D R1614 1K 5% 1/16W MF-LF 402

R1616 1K 5% 1/16W MF-LF 402

R1618 1K 5% 1/16W MF-LF 402

NO STUFF R1611 1K 5% 1/16W MF-LF 402

CPUPOC3D R1613 1K 5% 1/16W MF-LF 402

CPUPOC5D R1615 1K 5% 1/16W MF-LF 402

NO STUFF R1617 1K 5% 1/16W MF-LF 402

VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_20	20A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_20_30	30A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_30_40	40A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_40_50	50A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_50_60	60A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_60_70	70A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_70_90	90A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

86 73 70 40 26 25 24 23 21 20 18 17 PP1V05_S0

PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000.

C1653 C1654 C1655 C1656
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..

C1657 C1658 C1659 C1660 C1661 C1662 C1663
10UF 20% 6.3V X5R 603

PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.

C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675
1UF 10% 100V X5R 402

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686 C1687
1UF 10% 100V X5R 402

C1688 C1689 C1690
330UF 20% 2.0V POLY-TANT D2T-SM2

VTT0_DDR DECOUPLING

3x 1uF 0402

PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.

L1695
30-OHM-5A
0603

PP1V1R1V05_S0_CPU_VTT0_DDR 13
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

C1695 C1696 C1697
1UF 10% 100V X5R 402

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
CPU Non-GFX Decoupling (1 of 2)

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REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 16 OF 132
SHEET 15 OF 101

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VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP0

C1700 1UF 10% 16V X5R 402 | C1701 1UF 10% 16V X5R 402 | C1702 1UF 10% 16V X5R 402 | C1703 1UF 10% 16V X5R 402 | C1704 1UF 10% 16V X5R 402 | C1705 1UF 10% 16V X5R 402 | C1706 1UF 10% 16V X5R 402 | C1707 1UF 10% 16V X5R 402 | C1708 1UF 10% 16V X5R 402 | C1709 1UF 10% 16V X5R 402 | C1710 1UF 10% 16V X5R 402 | C1711 1UF 10% 16V X5R 402

VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP1

C1712 1UF 10% 16V X5R 402 | C1713 1UF 10% 16V X5R 402 | C1714 1UF 10% 16V X5R 402 | C1715 1UF 10% 16V X5R 402 | C1716 1UF 10% 16V X5R 402 | C1717 1UF 10% 16V X5R 402 | C1718 1UF 10% 16V X5R 402 | C1719 1UF 10% 16V X5R 402 | C1720 1UF 10% 16V X5R 402 | C1721 1UF 10% 16V X5R 402 | C1722 1UF 10% 16V X5R 402 | C1723 1UF 10% 16V X5R 402

Memory (CPU VCCDDR) DECOUPLING

5x 1uF 0402

NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.

42 31 16 13 7 6 99 73 72 PP1V5_S3RS0

C1724 1UF 10% 10V X5R 402 | C1725 1UF 10% 10V X5R 402 | C1726 1UF 10% 10V X5R 402 | C1727 1UF 10% 10V X5R 402 | C1728 1UF 10% 10V X5R 402

NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.

C1735 1UF 10% 10V X5R 402 | C1736 1UF 10% 10V X5R 402 | C1737 1UF 10% 10V X5R 402 | C1738 1UF 10% 10V X5R 402 | C1739 1UF 10% 10V X5R 402 | C1740 1UF 10% 10V X5R 402 | C1741 1UF 10% 10V X5R 402 | C1742 1UF 10% 10V X5R 402 | C1743 1UF 10% 10V X5R 402 | C1744 1UF 10% 10V X5R 402 | C1745 1UF 10% 10V X5R 402 | C1746 1UF 10% 10V X5R 402 | C1747 1UF 10% 10V X5R 402 | C1748 1UF 10% 10V X5R 402 | C1749 1UF 10% 10V X5R 402 | C1750 1UF 10% 10V X5R 402 | C1751 1UF 10% 10V X5R 402 | C1752 1UF 10% 10V X5R 402 | C1753 1UF 10% 10V X5R 402

C1729 330UF 20% 2.0V POLY-TANT D2T-SM2

PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

24 23 21 17 7 6 87 72 71 58 PP1V8_S0

C1732 22uF 20% 6.3V CERM-X5R 805 | C1733 4.7UF 10% 6.3V X5R-CERM 603

DDR Clock (CPU VDDQ_CK) DECOUPLING

1x 1uF 0402

42 31 16 13 7 6 99 73 72 PP1V5_S3RS0 — L1734 30-OHM-5A 0603 — PP1V5_S3_CPU_VCCDDR_CLK 12

C1734 1UF 10% 10V X5R 402

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC MASTER=K17 REF | SYNC DATE=06/15/2009

PAGE TITLE: CPU Non-GFX Decoupling (2 of 2)

Apple Inc.

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REVISION: <E4LABEL>

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PAGE: 17 OF 132

SHEET: 16 OF 101

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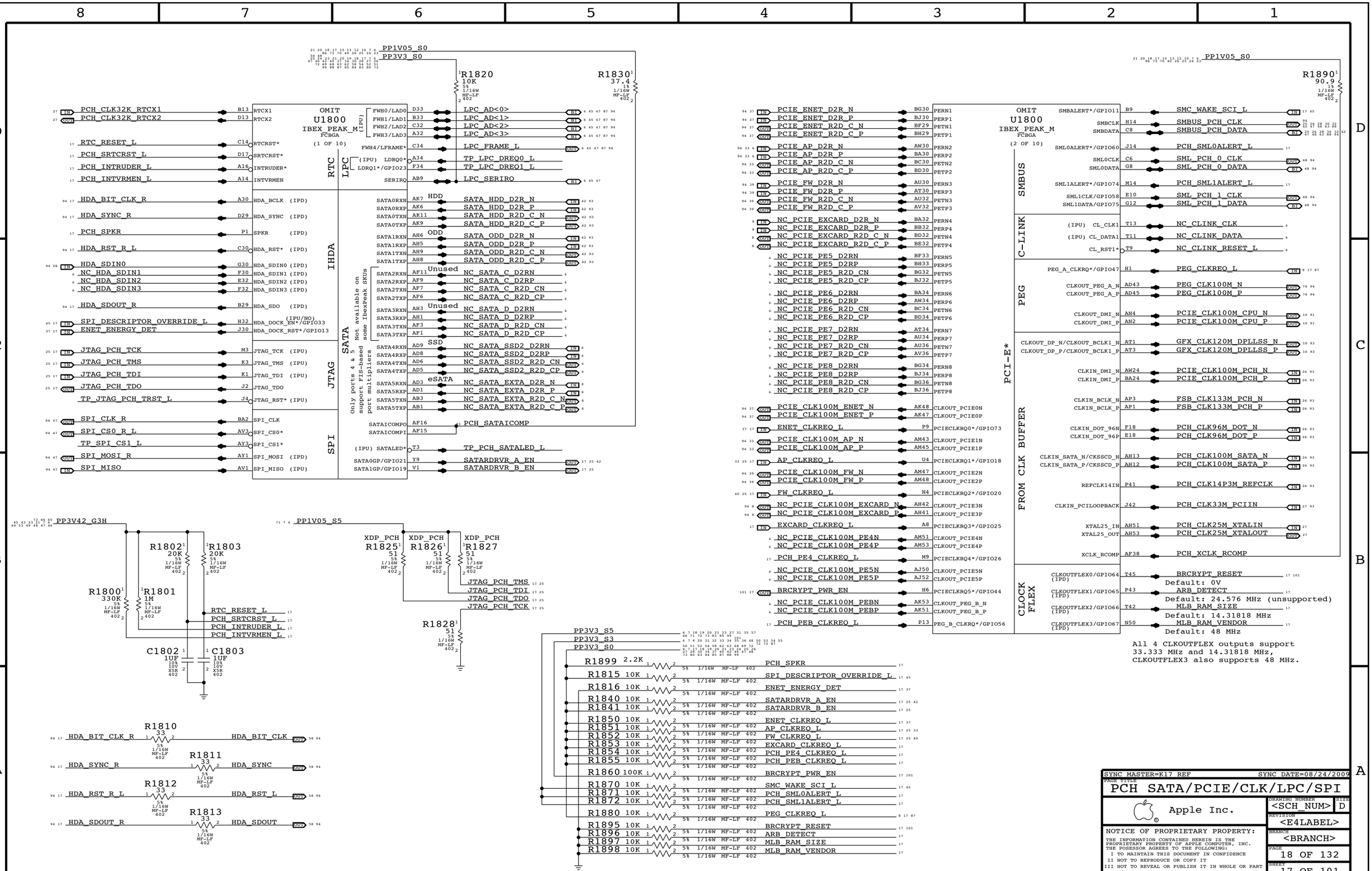

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PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

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PAGE 18 OF 132

SHEET 17 OF 101

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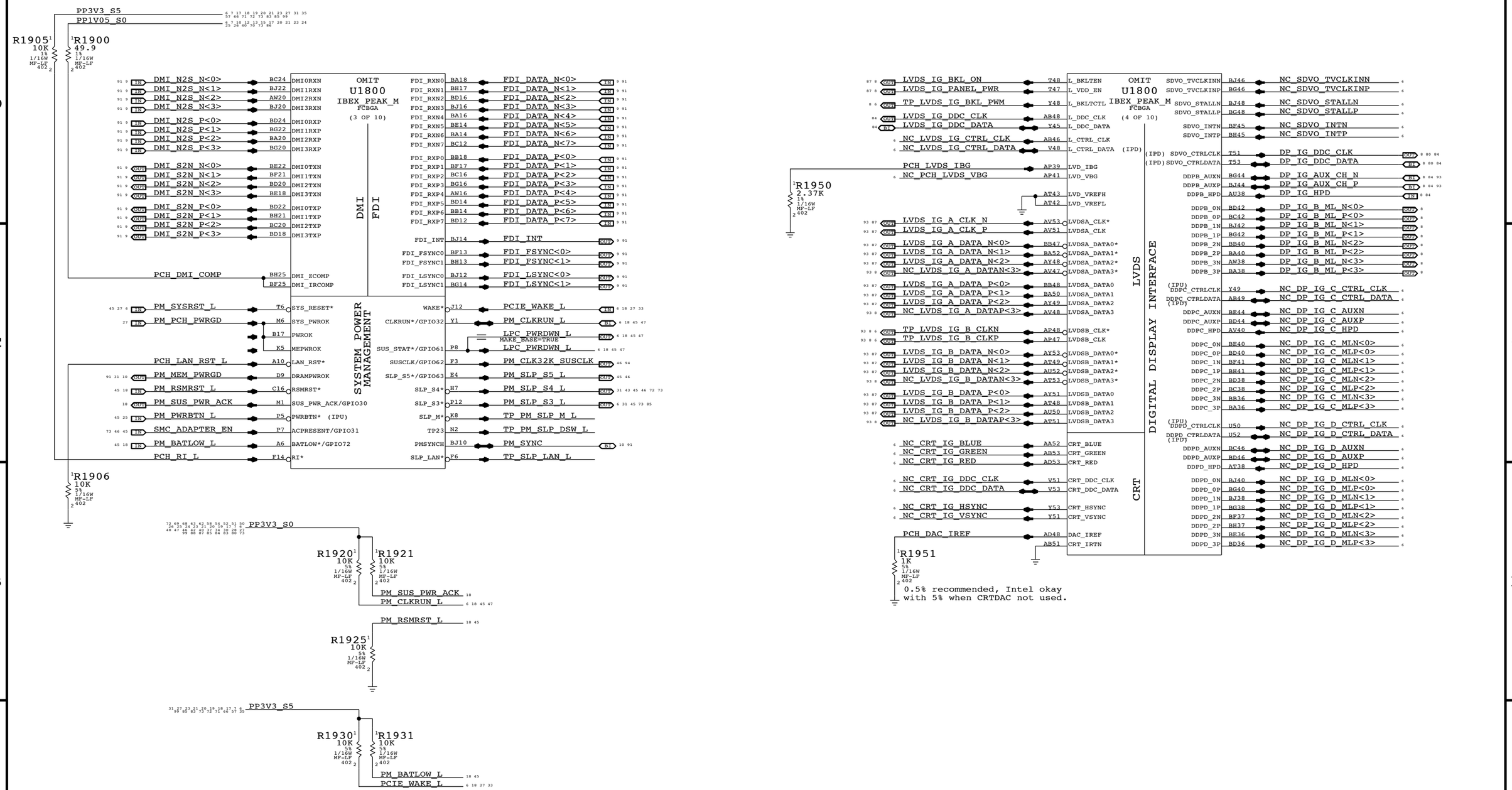

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PAGE TITLE
PCH DMI/FDI/Graphics

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PAGE 19 OF 132

SHEET 18 OF 101

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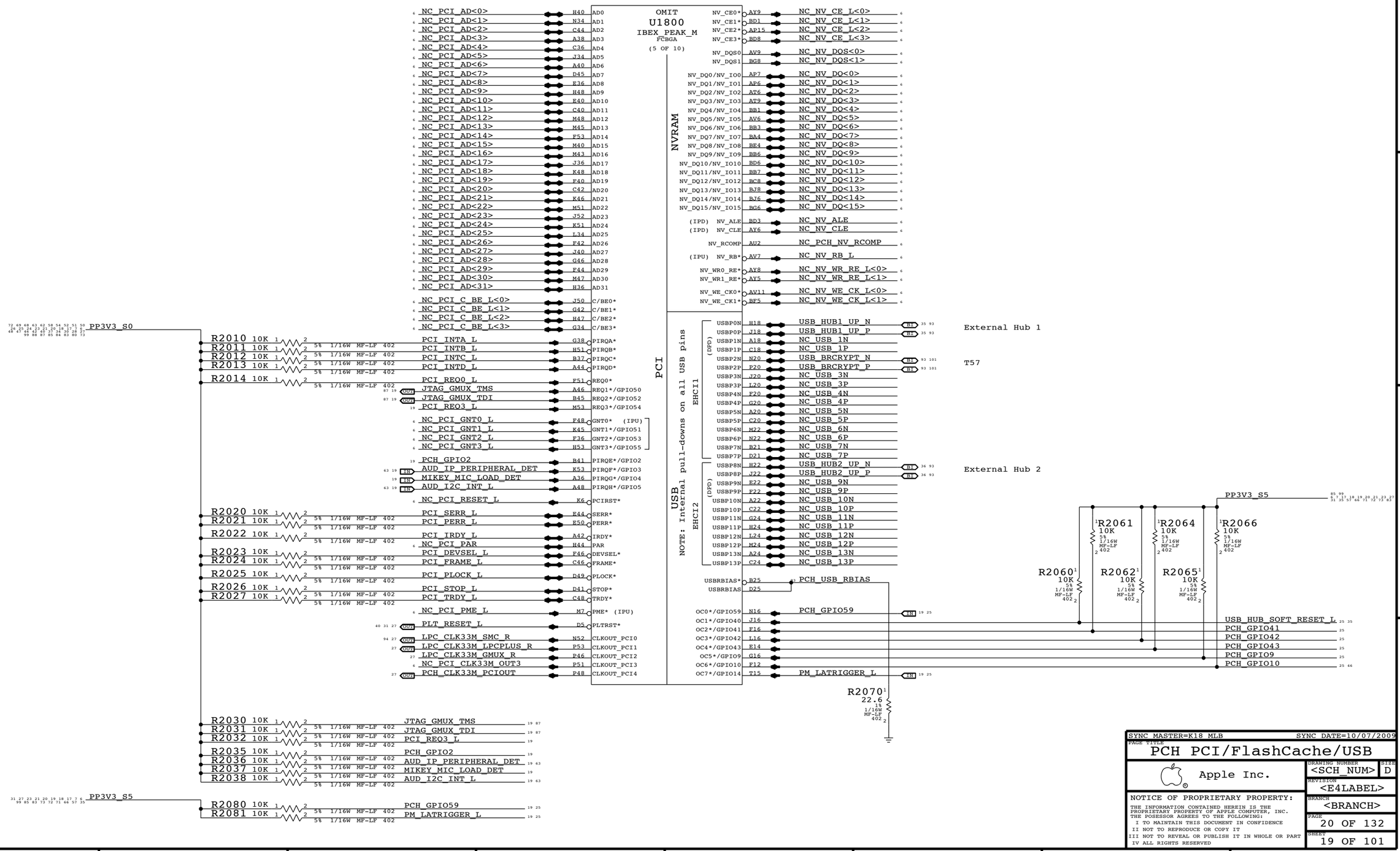

SYNC MASTER=K18 MLB SYNC DATE=10/07/2009

PAGE TITLE
PCH PCI/FlashCache/USB

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PAGE 20 OF 132

SHEET 19 OF 101

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IPU* = Only on TACH function.

OMIT
U1800
IBEX_PEAK_M
FCBGA
(6 OF 10)

46 45 25 20	IN	SMC_IG_THROTTLE_L	Y3	BMBUSY*/GPIO0	GPIO	
40 20 8	IN	FW_PLUG_DET_L	C38	TACH1/GPIO1 (IPU*)	GPIO	
87 20	IN	GMUX_INT	D37	TACH2/GPIO6 (IPU*)	GPIO	
45 20	IN	SMC_RUNTIME_SCI_L	J32	TACH3/GPIO7 (IPU*)	GPIO	
20		PCH_FCIM_EN_L	F10	GPIO8 (IPU)	GPIO	
37 20	OUT	ENET_LOW_PWR	K9	LAN_PHY_PWR_CTRL/GPIO12	GPIO	
20		PCH_GPIO15	T7	GPIO15 (IPD)	GPIO	
63 25 20	OUT	AUD_IPHS_SWITCH_EN	AA2	SATA4GP/GPIO16	GPIO	
47 20 6	BI	LPCPLUS_GPIO	F38	TACH0/GPIO17 (IPU*)	GPIO	
42 20	OUT	ODD_PWR_EN_L	Y7	SCLOCK/GPIO22	GPIO	
20		PCH_GPIO24	H10	MEM_LED/GPIO24	GPIO	
20		PCH_VRM_EN	AB12	GPIO27	GPIO	
31 25	OUT	ISOLATE_CPU_MEM_L	V13	GPIO28 (IPU)	GPIO	
		TP_PCH_STP_PCI_L	M11	STP_PCI*/GPIO34	GPIO	
20	OUT	MXM_GOOD	V6	SATACLKREQ*/GPIO35	GPIO	
34 25 20	OUT	SDCARD_RESET	AB7	SATA2GP/GPIO36	GPIO	
87 25 20	OUT	JTAG_GMUX_TCK	AB13	SATA3GP/GPIO37	GPIO	
87 20	IN	JTAG_GMUX_TDO	V3	SLOAD/GPIO38	GPIO	
20		PCH_GPIO39	P3	SDATAOUT0/GPIO39	GPIO	
73 20	OUT	WOL_EN	H3	PCIECLKRQ6*/GPIO45	GPIO	
73 33 20	OUT	AP_PWR_EN	F1	PCIECLKRQ7*/GPIO46	GPIO	
40 20	OUT	FW_PWR_EN	AB6	SDATAOUT1/GPIO48	GPIO	
25 20	OUT	ME_TEMP_ALERT_L	AA4	SATA5GP/GPIO49	GPIO	
57 47 20 6	BI	SPIROM_USE_MLB	F8	GPIO57	GPIO	
94 6		PCH_VSS_NCTF<1>	A4	VSS_NCTF1	NCTF	
94 6		PCH_VSS_NCTF<2>	A49	VSS_NCTF2	NCTF	
			A5	VSS_NCTF3	NCTF	
			A50	VSS_NCTF4	NCTF	
94 6		PCH_VSS_NCTF<5>	A52	VSS_NCTF5	NCTF	
			A53	VSS_NCTF6	NCTF	
94		TP_PCH_VSS_NCTF<7>	B2	VSS_NCTF7	NCTF	
			B4	VSS_NCTF8	NCTF	
94 6		PCH_VSS_NCTF<9>	B52	VSS_NCTF9	NCTF	
			B53	VSS_NCTF10	NCTF	
94 6		PCH_VSS_NCTF<11>	BE1	VSS_NCTF11	NCTF	
94 6		PCH_VSS_NCTF<12>	BE53	VSS_NCTF12	NCTF	
			BF1	VSS_NCTF13	NCTF	
			BF53	VSS_NCTF14	NCTF	
94 6		PCH_VSS_NCTF<15>	BH1	VSS_NCTF15	NCTF	
			BH2	VSS_NCTF16	NCTF	
94 6		PCH_VSS_NCTF<17>	BH52	VSS_NCTF17	NCTF	
			BH53	VSS_NCTF18	NCTF	
94 6		PCH_VSS_NCTF<19>	BJ1	VSS_NCTF19	NCTF	
			BJ2	VSS_NCTF20	NCTF	
94 6		PCH_VSS_NCTF<21>	BJ4	VSS_NCTF21	NCTF	
94		PCH_VSS_NCTF<22>	BJ49	VSS_NCTF22	NCTF	
			BJ5	VSS_NCTF23	NCTF	
			BJ50	VSS_NCTF24	NCTF	
94 6		PCH_VSS_NCTF<25>	BJ52	VSS_NCTF25	NCTF	
			BJ53	VSS_NCTF26	NCTF	
94 6		PCH_VSS_NCTF<27>	D1	VSS_NCTF27	NCTF	
			D2	VSS_NCTF28	NCTF	
94 6		PCH_VSS_NCTF<29>	D53	VSS_NCTF29	NCTF	
			E1	VSS_NCTF30	NCTF	
			E53	VSS_NCTF31	NCTF	

	CLKOUT_PCIE6N	AH45	NC_PCIE_CLK100M_PE6N	6	
	CLKOUT_PCIE6P	AH46	NC_PCIE_CLK100M_PE6P	6	
	CLKOUT_PCIE7N	AF48	NC_PCIE_CLK100M_PE7N	6	
	CLKOUT_PCIE7P	AF47	NC_PCIE_CLK100M_PE7P	6	
MISC	A20GATE	U2	PCH_A20GATE		
CPU	CLKOUT_BCLK0_N/CLKOUT_PCIE8N	AM3	FSB_CLK133M_CPU_N	OUT 10 91	
CPU	CLKOUT_BCLK0_P/CLKOUT_PCIE8P	AM1	FSB_CLK133M_CPU_P	OUT 10 91	
CPU	PECI	BG10	CPU_PECI	BI 10 91	
CPU	RCIN*	T1	PCH_RCIN_L		
CPU	PROCPWRGD	BE10	CPU_PWRGD	OUT 10 25 91	
CPU	THRMTRIP*	BD10	PCH_THRMTRIP_L		
RSVD	TP1	BA22	NC_PCH_TP1	6	
RSVD	TP2	AW22	NC_PCH_TP2	6	
RSVD	TP3	BB22	NC_PCH_TP3	6	
RSVD	TP4	AY45	NC_PCH_TP4	6	(DPL_B_MON1_N)
RSVD	TP5	AY46	NC_PCH_TP5	6	(DPL_B_MON1_P)
RSVD	TP6	AV43	NC_PCH_TP6	6	(DPL_B_MON2_N)
RSVD	TP7	AV45	NC_PCH_TP7	6	(DPL_B_MON2_P)
RSVD	TP8	AF13	NC_PCH_TP8	6	(SATA_OB_ANA)
RSVD	TP9	M18	NC_PCH_TP9	6	
RSVD	TP10	N18	NC_PCH_TP10	6	
RSVD	TP11	AJ24	NC_PCH_TP11	6	
RSVD	TP12	AK41	NC_PCH_TP12	6	(XCKPLL_MON1_N)
RSVD	TP13	AK42	NC_PCH_TP13	6	(XCKPLL_MON1_P)
RSVD	TP14	M32	NC_PCH_TP14	6	
RSVD	TP15	N32	NC_PCH_TP15	6	
RSVD	TP16	M30	NC_PCH_TP16	6	
RSVD	TP17	N30	NC_PCH_TP17	6	
RSVD	TP18	H12	NC_PCH_TP18	6	
RSVD	TP19	AA23	NC_PCH_TP19	6	
RSVD	NC_1	AB45	NC_PCH_NC1	6	
RSVD	NC_2	AB38	NC_PCH_NC2	6	
RSVD	NC_3	AB42	NC_PCH_NC3	6	
RSVD	NC_4	AB41	NC_PCH_NC4	6	
RSVD	NC_5	T39	NC_PCH_NC5	6	
RSVD	(IPD) INIT3_3V*	P6	TP_PCH_INIT3V3_L		
RSVD	TP24	C10	NC_PCH_SST	6	

PP3V3_S0 — 50 51 52 54 58 62 63 68 69 72 6 7 17 18 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48 73 80 83 84 85 87 88 99

R2150 10K 5% 1/16W MF-LF 402 (1–2)

R2155 10K 5% 1/16W MF-LF 402 (1–2)

PP1V05_S0 — 6 7 10 12 13 15 17 18 21 23 24 25 26 40 70 73 86

R2160 56 5% 1/16W MF-LF 402 (1–2)

R2161 56 5% 1/16W MF-LF 402 (1–2)

PM_THRMTRIP_L — IN 10 46 91

PP3V3_S5 — 6 7 17 18 19 21 23 27 31 35 57 66 72 73 85 89

PP3V3_S3 — 101 6 7 8 17 31 32 33 34 35 36 48 50 53 54 55

PP3V3_S0 — 50 51 52 54 58 62 63 68 69 72 72 73 87 6 7 17 18 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48 73 80 83 84 85 87 88 99

R2110	10K 5% 1/16W MF-LF 402	SMC_IG_THROTTLE_L	20 25 45 46	R2130	10K 5% 1/16W MF-LF 402
R2111	10K 5% 1/16W MF-LF 402	FW_PLUG_DET_L	8 20 40	R2131	10K 5% 1/16W MF-LF 402
R2112	20K 5% 1/16W MF-LF 402	GMUX_INT	20 87	R2132	10K 5% 1/16W MF-LF 402
R2113	10K 5% 1/16W MF-LF 402	SMC_RUNTIME_SCI_L	20 45	R2133	10K 5% 1/16W MF-LF 402
R2114	10K 5% 1/16W MF-LF 402	PCH_FCIM_EN_L	20	R2134	10K 5% 1/16W MF-LF 402
R2115	2.2K 5% 1/16W MF-LF 402	ENET_LOW_PWR	20 37	R2135	10K 5% 1/16W MF-LF 402
R2116	10K 5% 1/16W MF-LF 402	PCH_GPIO15	20	R2136	10K 5% 1/16W MF-LF 402
R2120	10K 5% 1/16W MF-LF 402	AUD_IPHS_SWITCH_EN	20 25 63	R2137	10K 5% 1/16W MF-LF 402
R2121	10K 5% 1/16W MF-LF 402	LPCPLUS_GPIO	6 20 47	R2138	10K 5% 1/16W MF-LF 402
R2122	10K 5% 1/16W MF-LF 402	ODD_PWR_EN_L	20 42	R2139	100K 5% 1/16W MF-LF 402
R2123	10K 5% 1/16W MF-LF 402	PCH_GPIO24	20		
R2124	10K 5% 1/16W MF-LF 402	PCH_VRM_EN	20		
R2130	10K 5% 1/16W MF-LF 402	MXM_GOOD	20		
R2131	10K 5% 1/16W MF-LF 402	SDCARD_RESET	20 25 34		
R2132	10K 5% 1/16W MF-LF 402	JTAG_GMUX_TCK	20 25 87		
R2133	10K 5% 1/16W MF-LF 402	JTAG_GMUX_TDO	20 87		
R2134	10K 5% 1/16W MF-LF 402	PCH_GPIO39	20		
R2135	10K 5% 1/16W MF-LF 402	WOL_EN	20 73		
R2136	10K 5% 1/16W MF-LF 402	AP_PWR_EN	20 33 73		
R2137	10K 5% 1/16W MF-LF 402	FW_PWR_EN	20 40		
R2138	10K 5% 1/16W MF-LF 402	ME_TEMP_ALERT_L	20 25		
R2139	100K 5% 1/16W MF-LF 402	SPIROM_USE_MLB	6 20 47 57		

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PAGE TITLE: PCH MISC

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PAGE: 21 OF 132

SHEET: 20 OF 101

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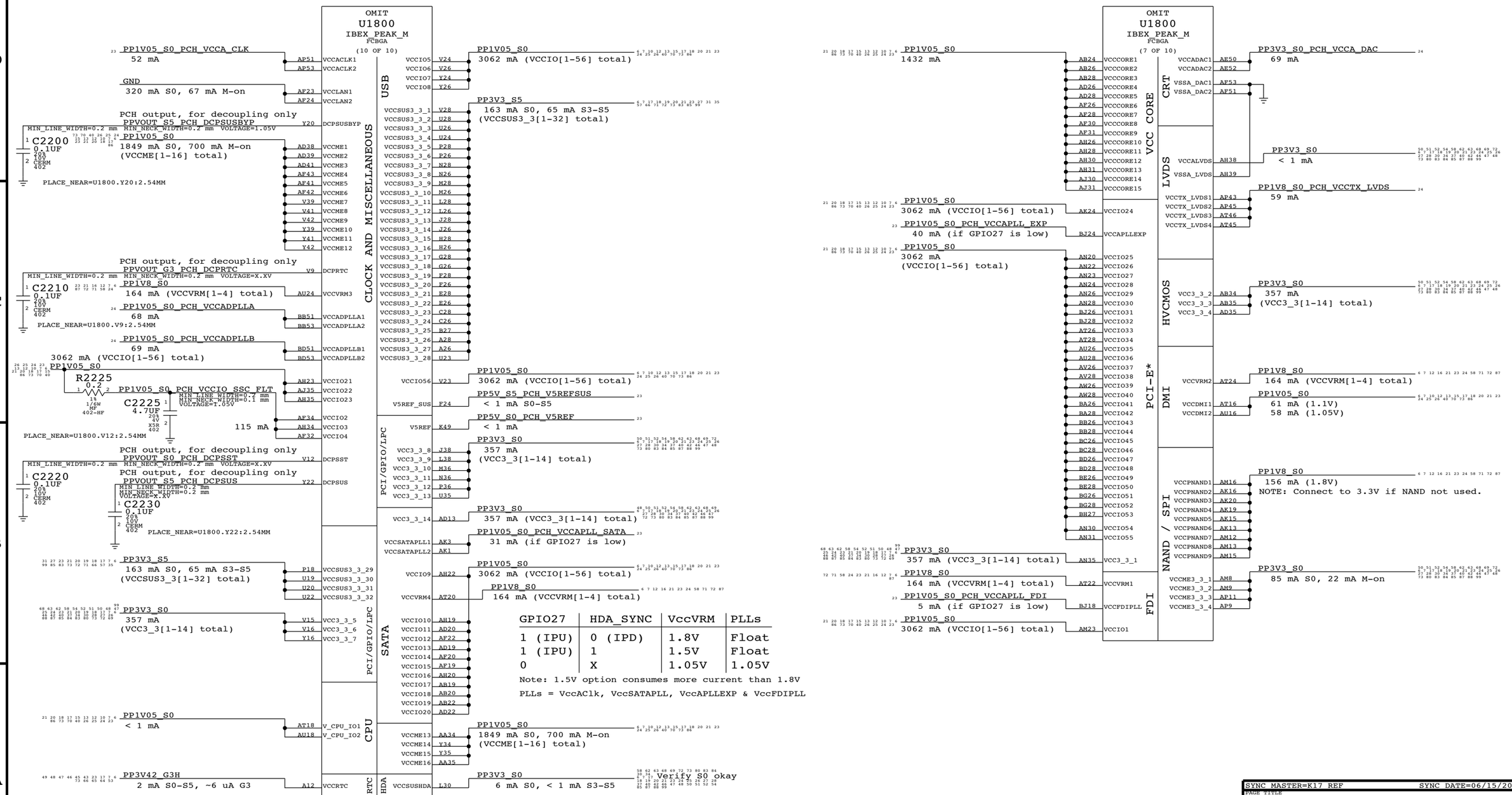

GPIO27	HDA_SYNC	VccVRM	PLLs
1 (IPU)	0 (IPD)	1.8V	Float
1 (IPU)	1	1.5V	Float
0	X	1.05V	1.05V

Note: 1.5V option consumes more current than 1.8V

PLLs = VccAClk, VccSATAPLL, VccAPLLEXP & VccFDIPLL

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

PCH Power

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PAGE 22 OF 132

SHEET 21 OF 101

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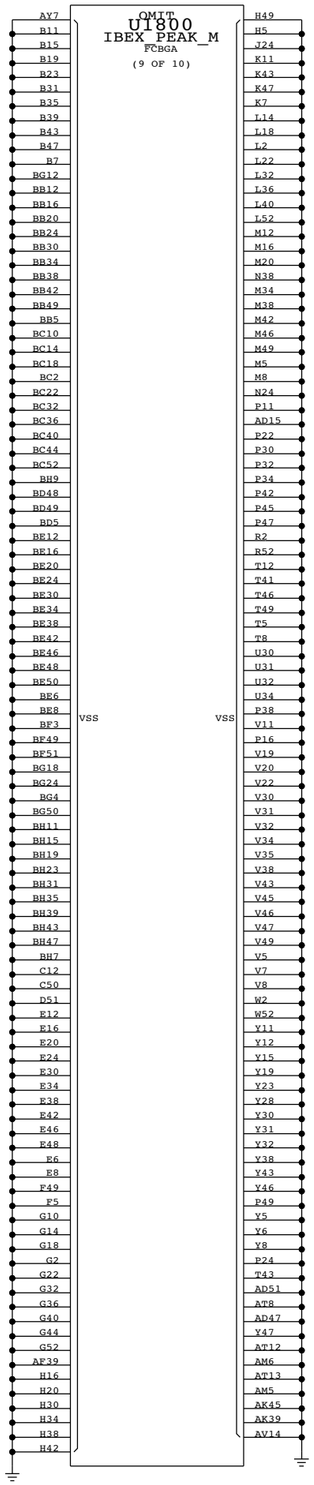

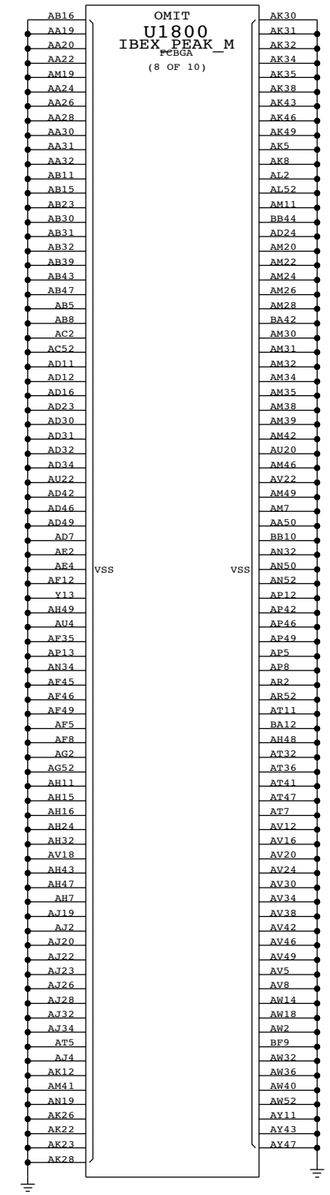

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PAGE TITLE

PCH Grounds

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PAGE 23 OF 132

SHEET 22 OF 101

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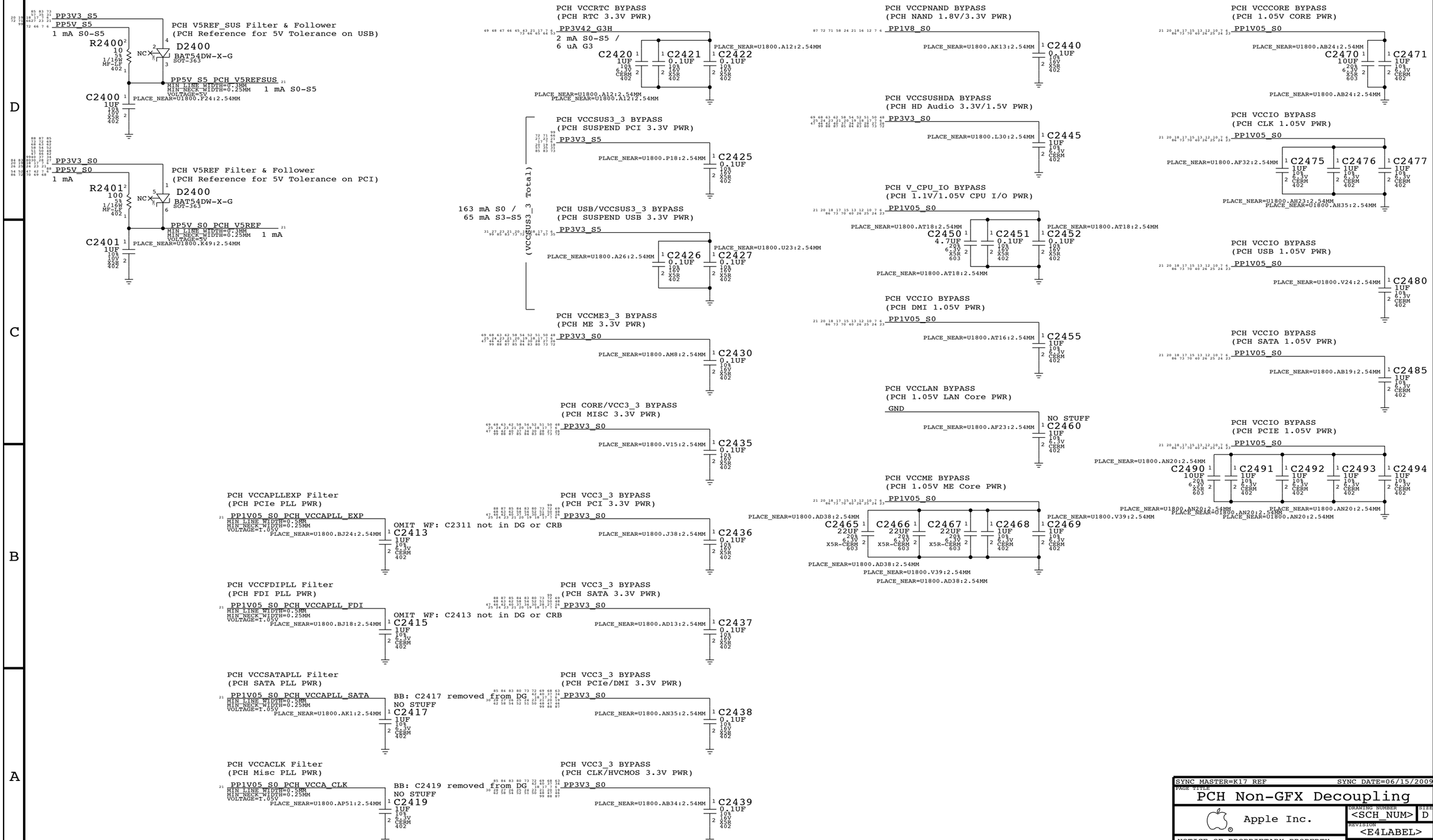

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
PCH Non-GFX Decoupling

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PAGE 24 OF 132

SHEET 23 OF 101

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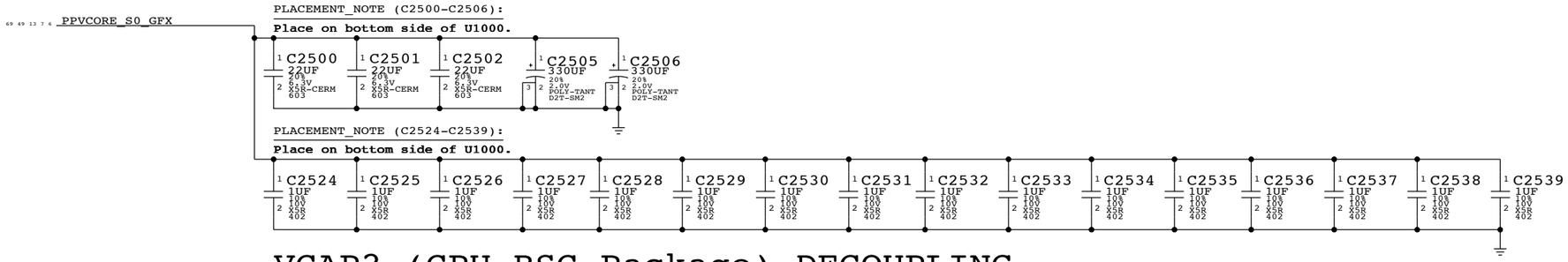
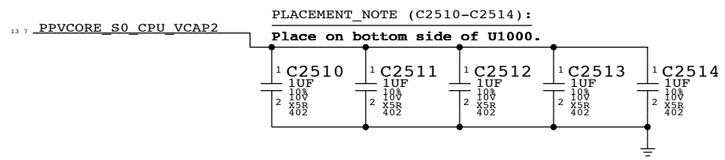
GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

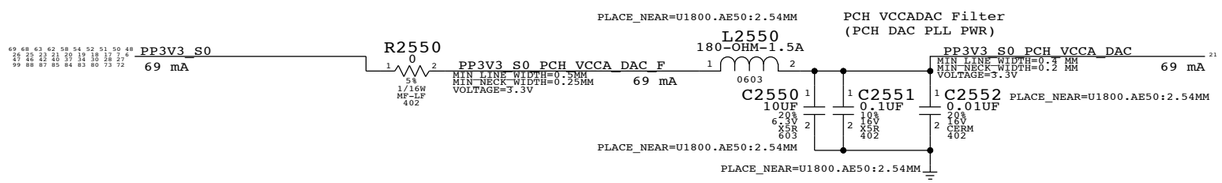


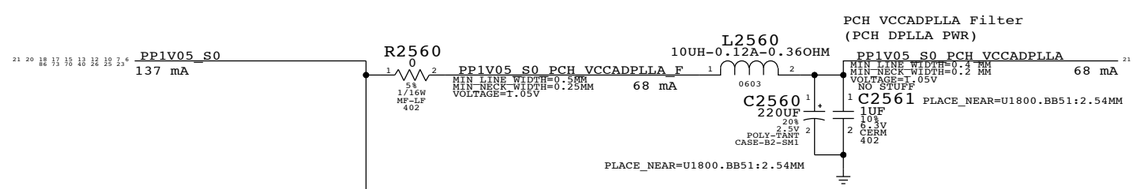
VCAP2 (CPU BSC Package) DECOUPLING

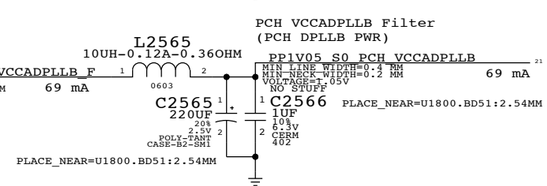
5x 1uF 0402

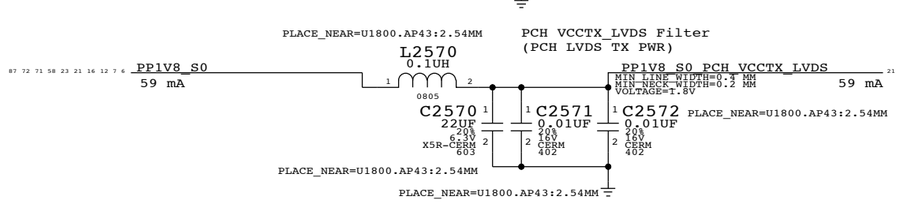


Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.









Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
CPU/PCH GFX Decoupling

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PAGE 25 OF 132

SHEET 24 OF 101

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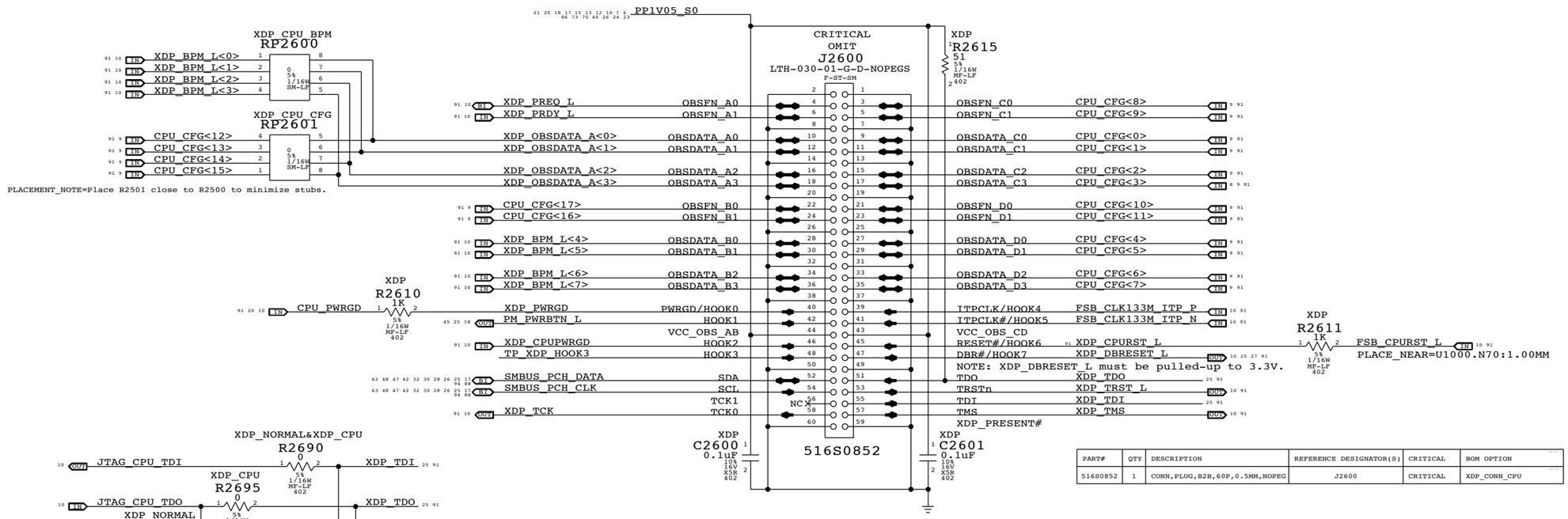
Calpella Processor mini XDP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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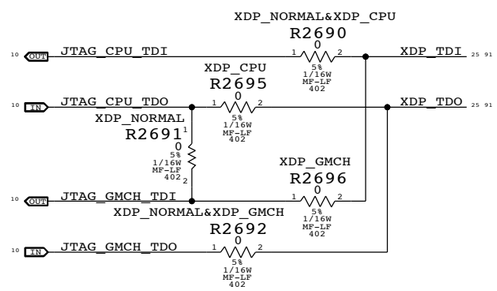
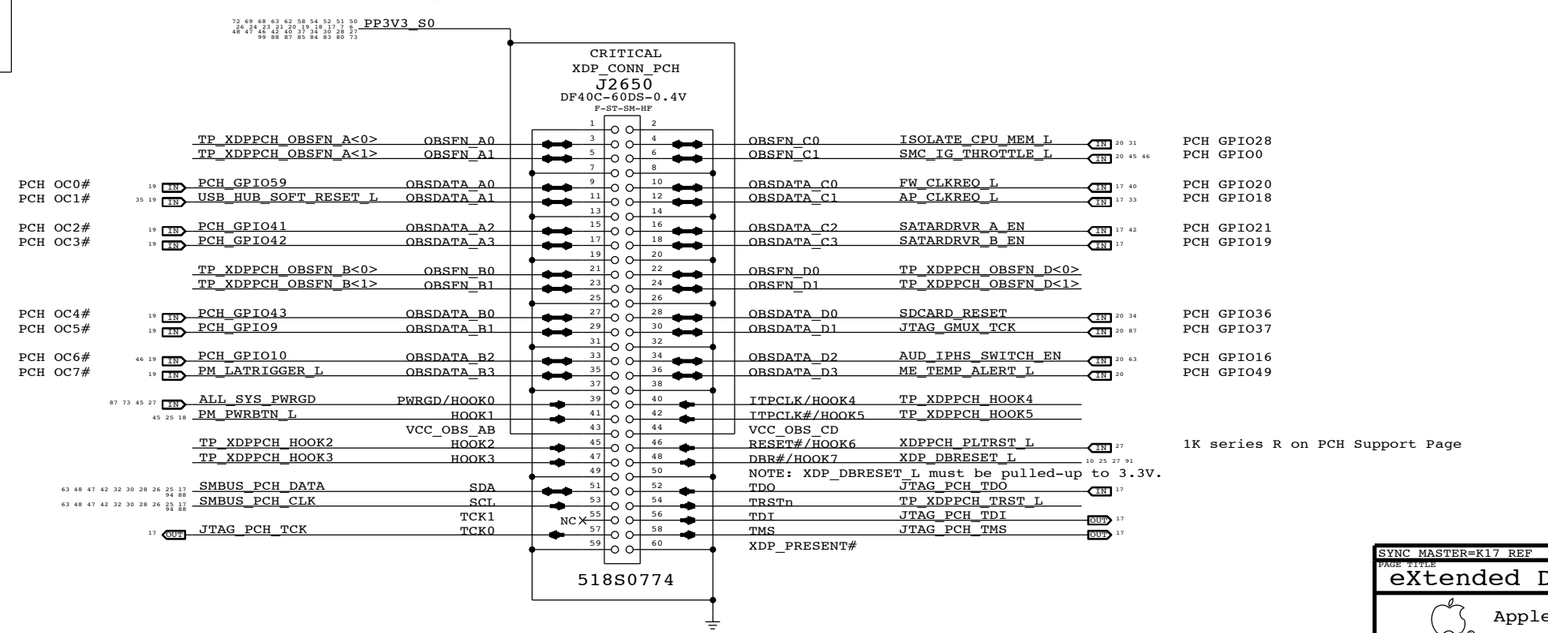


Calpella PCH mini XDP



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

eXtended Debug Port (XDP)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 26 OF 132

SHEET 25 OF 101

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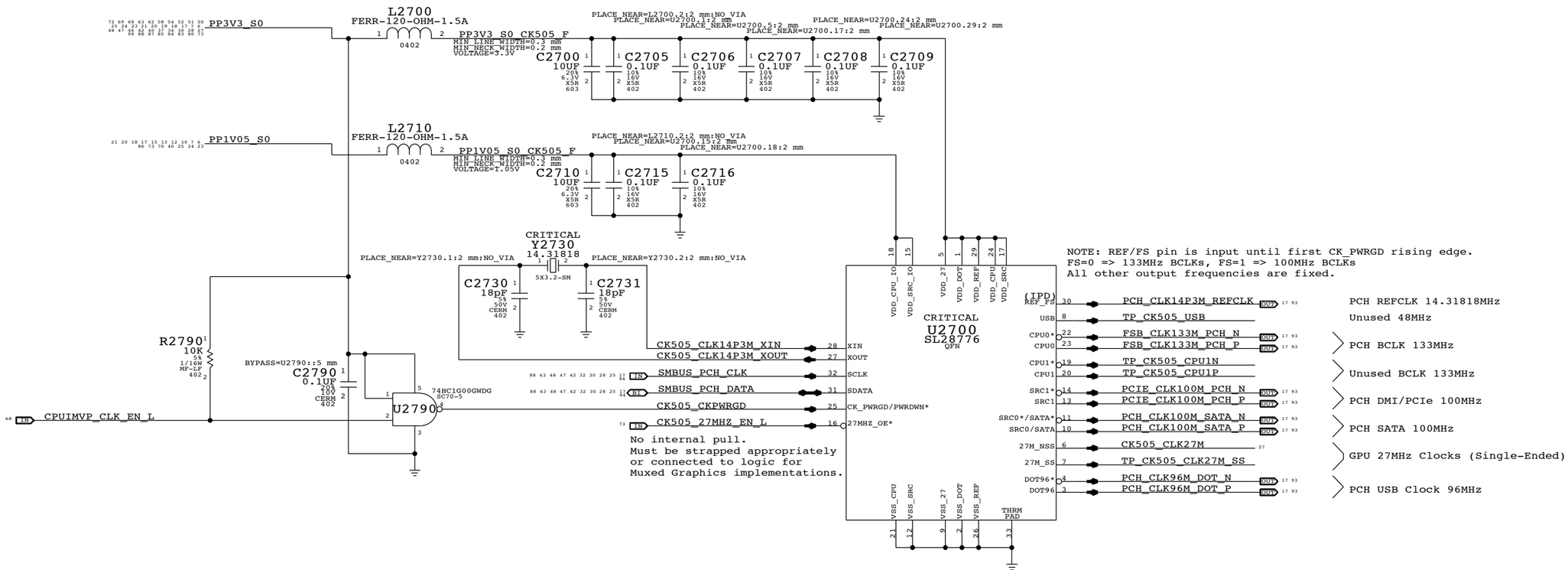

SYNC MASTER=K17 MLB SYNC DATE=06/23/2009

PAGE TITLE

Clock (CK505)

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DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 27 OF 132

SHEET 26 OF 101

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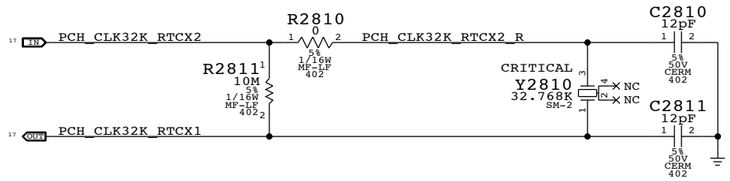
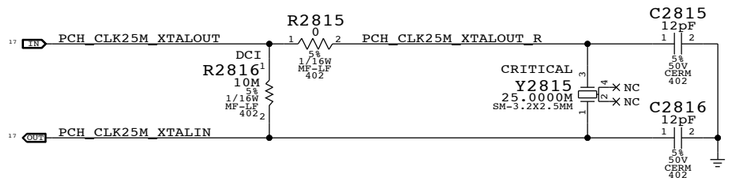
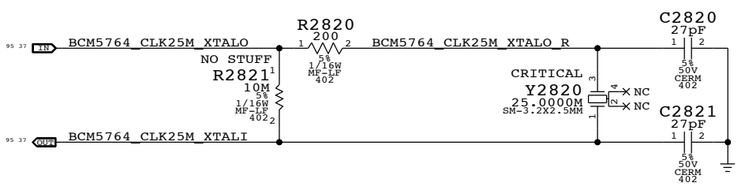
PCH RTC Crystal



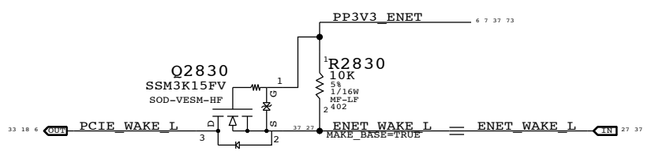
PCH 25MHz Crystal



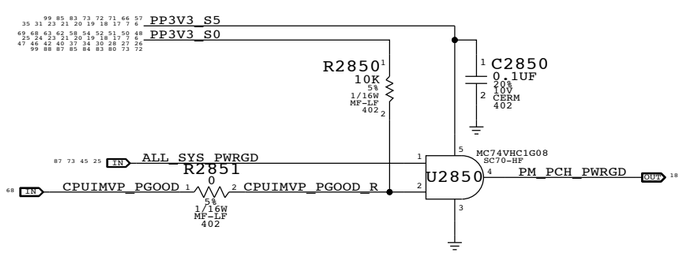
Caesar II (ENET) 25MHz Crystal



Ethernet WAKE# Isolation

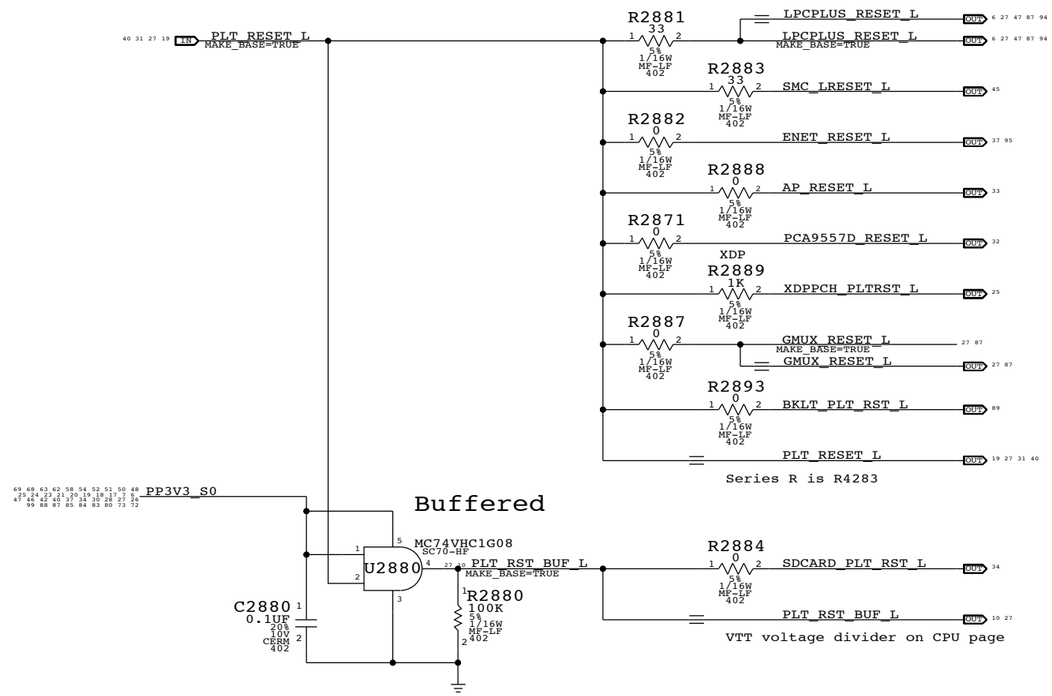


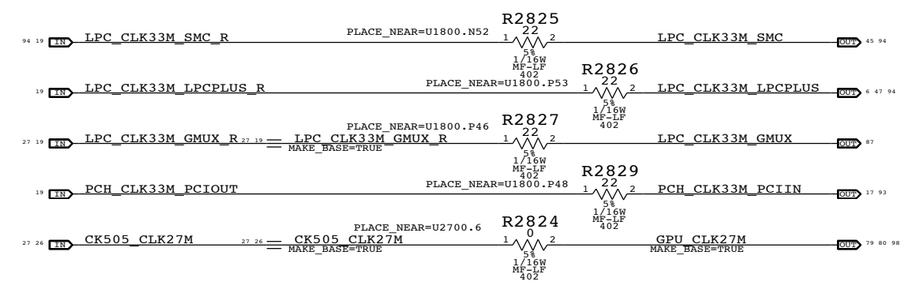
PCH S0 PWRGD



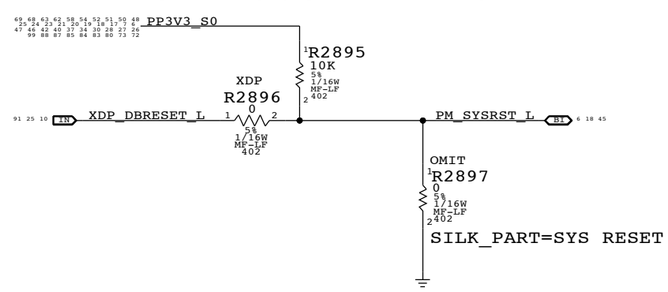
Platform Reset Connections

Unbuffered





PCH Reset Button



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 28 OF 132

SHEET 27 OF 101

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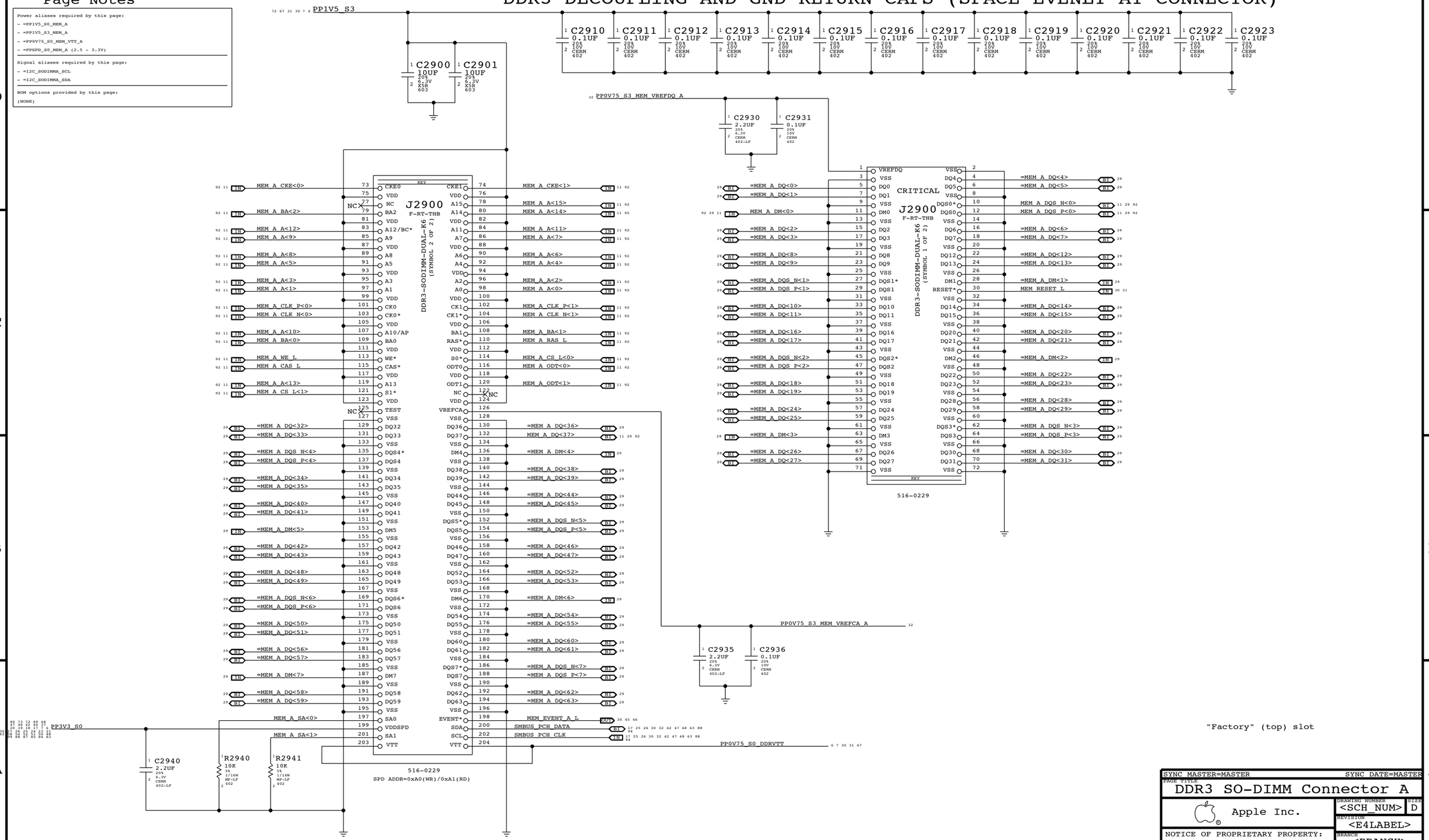
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE 29 OF 132

SHEET 28 OF 101

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92 29 28 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	MEM_A_DQS_N<0>	11 28 29 92 92 30 29 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	MEM_B_DQS_N<0> 11 29 30 92
92 29 28 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	MEM_A_DQS_P<0>	11 28 29 92 92 30 29 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	MEM_B_DQS_P<0> 11 29 30 92
92 29 28 11	MEM_A_DM<0>	MAKE_BASE=TRUE	MEM_A_DM<0>	11 28 29 92 92 30 29 11	MEM_B_DM<0>	MAKE_BASE=TRUE	MEM_B_DM<0> 11 29 30 92
92 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7> 28	92 11	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7> 30
92 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6> 28	92 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6> 30
92 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<1> 28	92 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<2> 30
92 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<0> 28	92 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4> 30
92 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<2> 28	92 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3> 30
92 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<3> 28	92 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<1> 30
92 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<5> 28	92 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5> 30
92 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<4> 28	92 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 1 -> DIMM A DQS 1 / CPU CHANNEL B DQS 1 -> DIMM B DQS 1

92 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1> 28	92 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1> 30
92 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1> 28	92 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1> 30
92 11	MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<1> 28	92 11	MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<1> 30
92 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<11> 28	92 11	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15> 30
92 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<10> 28	92 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14> 30
92 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<8> 28	92 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13> 30
92 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<9> 28	92 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<8> 30
92 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<15> 28	92 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11> 30
92 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<14> 28	92 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10> 30
92 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<13> 28	92 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<12> 30
92 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<12> 28	92 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<9> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 2 -> DIMM A DQS 2 / CPU CHANNEL B DQS 2 -> DIMM B DQS 2

92 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2> 28	92 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2> 30
92 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2> 28	92 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2> 30
92 11	MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<2> 28	92 11	MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<2> 30
92 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23> 28	92 11	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23> 30
92 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<19> 28	92 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<18> 30
92 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<20> 28	92 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<20> 30
92 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<22> 28	92 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<17> 30
92 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<21> 28	92 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19> 30
92 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18> 28	92 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<22> 30
92 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17> 28	92 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<21> 30
92 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16> 28	92 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 3 -> DIMM A DQS 3 / CPU CHANNEL B DQS 3 -> DIMM B DQS 3

92 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3> 28	92 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3> 30
92 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3> 28	92 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3> 30
92 11	MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<3> 28	92 11	MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<3> 30
92 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<27> 28	92 11	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<27> 30
92 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<26> 28	92 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<26> 30
92 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<25> 28	92 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<24> 30
92 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<24> 28	92 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<30> 30
92 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<31> 28	92 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<28> 30
92 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<30> 28	92 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<29> 30
92 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<28> 28	92 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<31> 30
92 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<29> 28	92 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<25> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 4 -> DIMM A DQS 4 / CPU CHANNEL B DQS 4 -> DIMM B DQS 4

92 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4> 28	92 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4> 30
92 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4> 28	92 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4> 30
92 11	MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<4> 28	92 11	MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<4> 30
92 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<33> 28	92 11	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<35> 30
92 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<39> 28	92 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38> 30
92 29 28 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	MEM_A_DQ<37> 11 28 29 92 92 30 29 11	92 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	MEM_B_DQ<37> 11 29 30 92
92 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<38> 28	92 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<32> 30
92 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35> 28	92 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<33> 30
92 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34> 28	92 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<39> 30
92 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32> 28	92 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<37> 30
92 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<36> 28	92 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<36> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 5 -> DIMM A DQS 5 / CPU CHANNEL B DQS 5 -> DIMM B DQS 5

92 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5> 28	92 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5> 30
92 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5> 28	92 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5> 30
92 11	MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<5> 28	92 11	MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<5> 30
92 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<43> 28	92 11	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47> 30
92 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<42> 28	92 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<43> 30
92 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45> 28	92 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45> 30
92 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44> 28	92 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<41> 30
92 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<47> 28	92 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<46> 30
92 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<46> 28	92 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42> 30
92 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<40> 28	92 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<44> 30
92 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<41> 28	92 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 6 -> DIMM A DQS 6 / CPU CHANNEL B DQS 6 -> DIMM B DQS 6

92 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6> 28	92 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6> 30
92 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6> 28	92 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6> 30
92 11	MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<6> 28	92 11	MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<6> 30
92 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<49> 28	92 11	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<50> 30
92 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<50> 28	92 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<55> 30
92 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<54> 28	92 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<54> 30
92 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<53> 28	92 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<53> 30
92 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<55> 28	92 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<49> 30
92 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<51> 28	92 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<51> 30
92 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<48> 28	92 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<48> 30
92 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<52> 28	92 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<52> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

CPU CHANNEL A DQS 7 -> DIMM A DQS 7 / CPU CHANNEL B DQS 7 -> DIMM B DQS 7

92 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7> 28	92 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7> 30
92 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7> 28	92 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7> 30
92 11	MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<7> 28	92 11	MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<7> 30
92 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<62> 28	92 11	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63> 30
92 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<63> 28	92 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62> 30
92 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<56> 28	92 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<57> 30
92 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<61> 28	92 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<56> 30
92 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59> 28	92 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59> 30
92 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58> 28	92 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58> 30
92 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57> 28	92 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<60> 30
92 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60> 28	92 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<61> 30
		MAKE_BASE=TRUE				MAKE_BASE=TRUE	

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 30 OF 132

SHEET 29 OF 101

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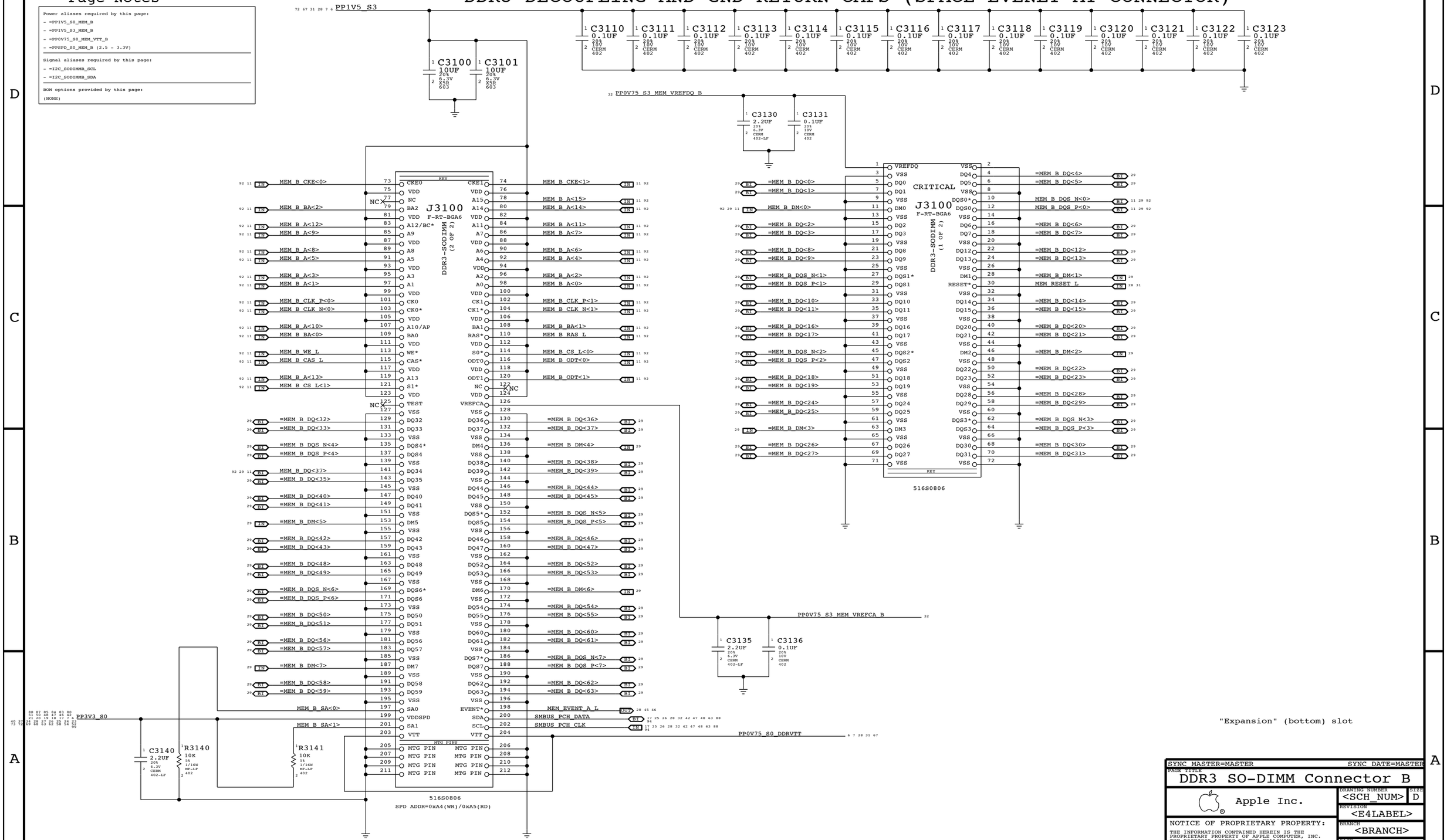
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)



SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 31 OF 132

SHEET: 30 OF 101

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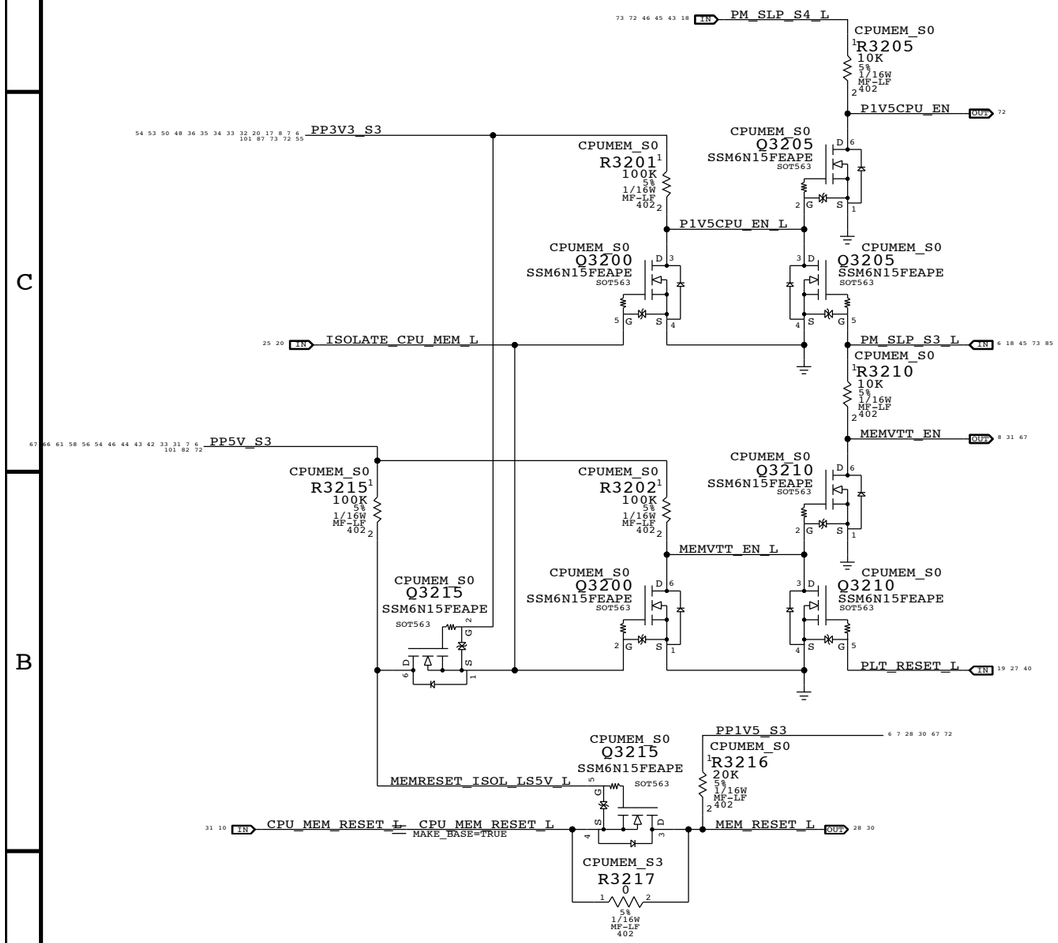
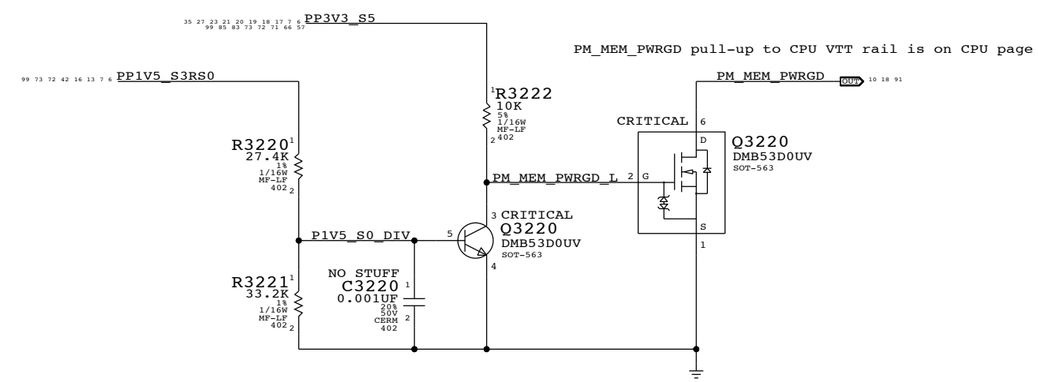
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

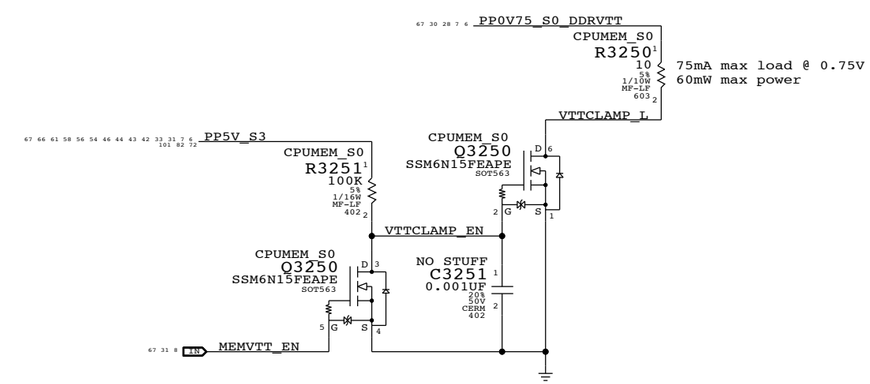


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 32 OF 132
SHEET 31 OF 101

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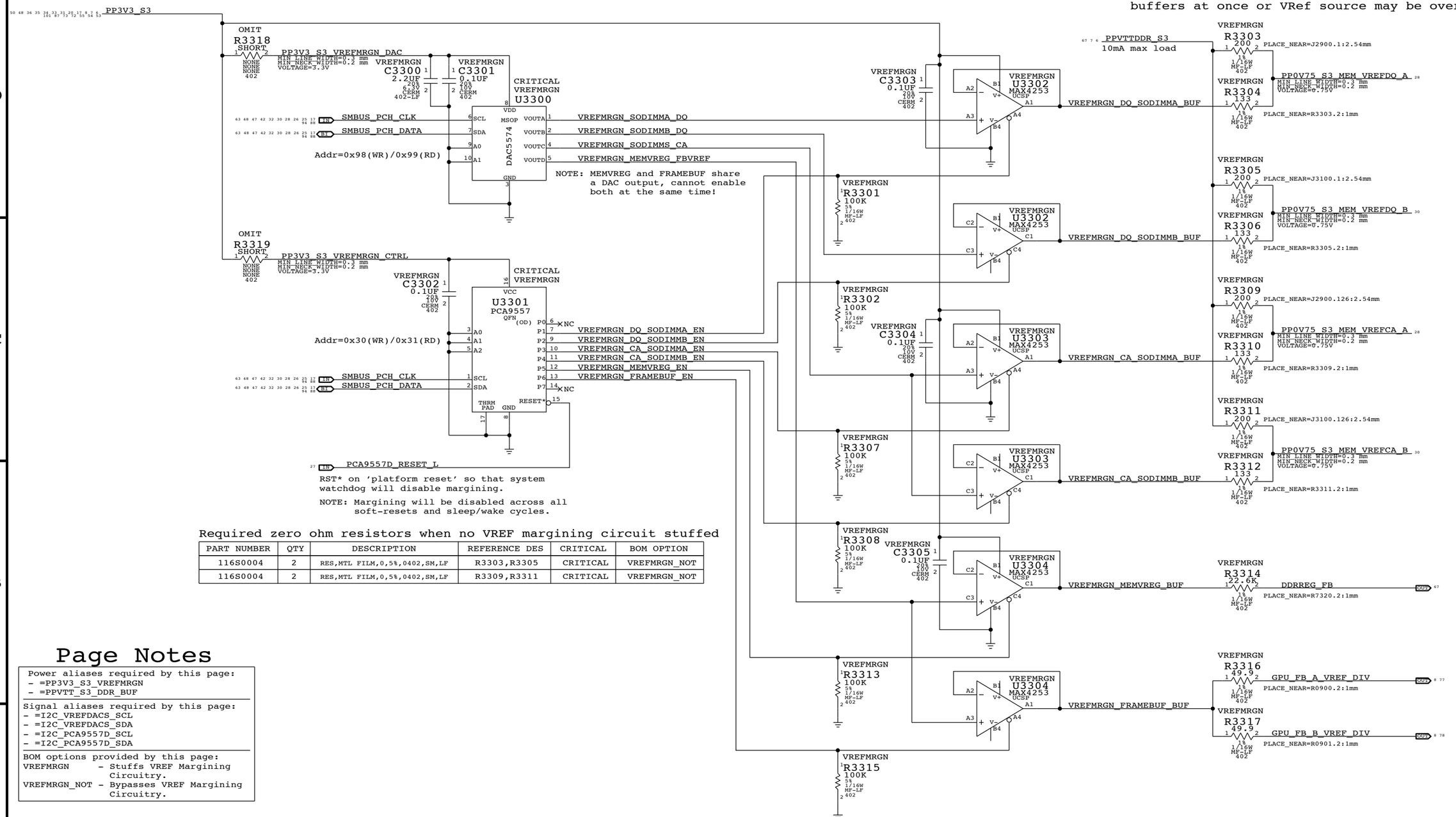
NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305	CRITICAL	VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311	CRITICAL	VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 33 OF 132
SHEET 32 OF 101

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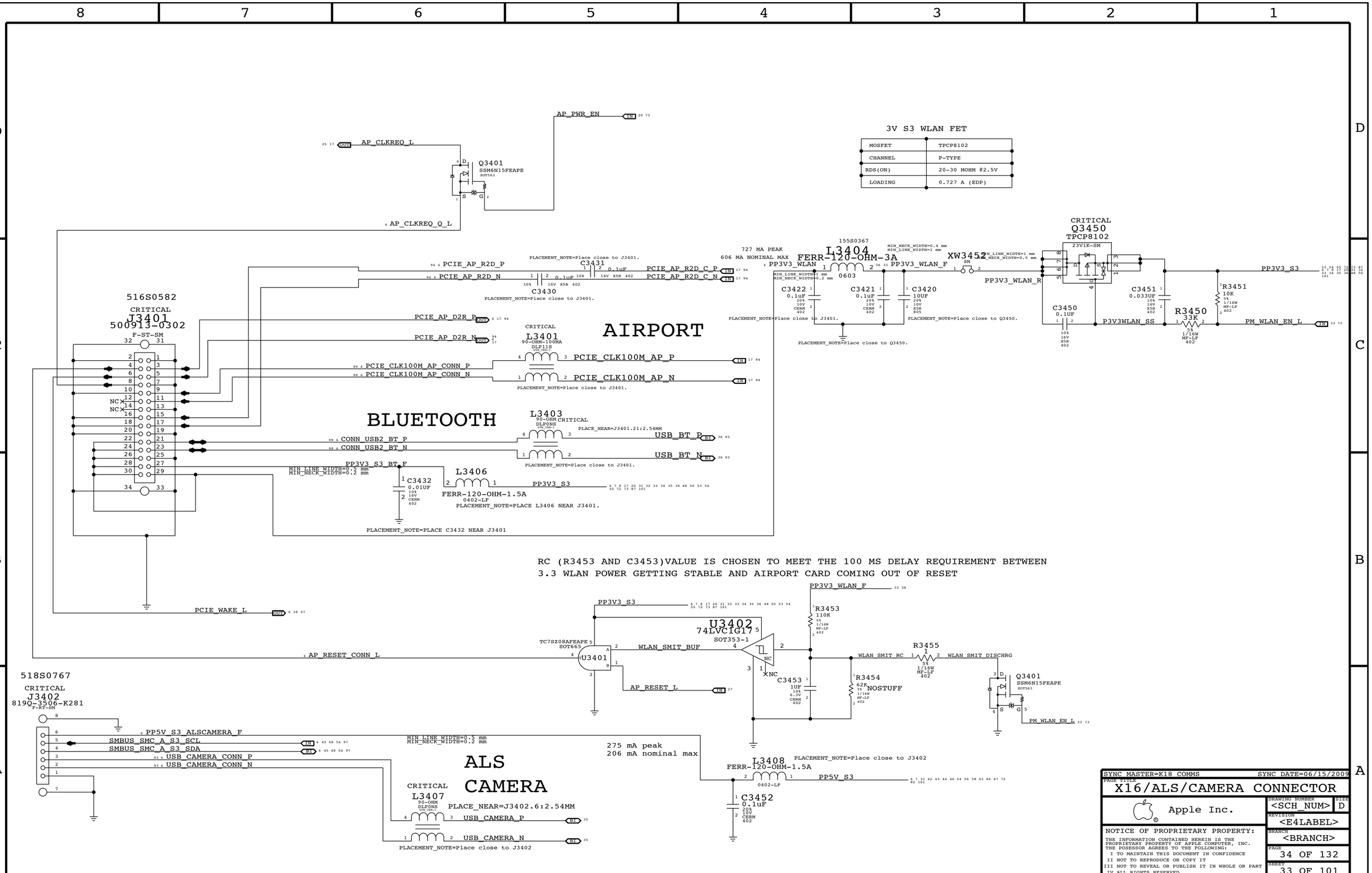
AP_PWR_EN
AP_CLKREQ_L
Q3401
SSM6N15FEAPE
AP_CLKREQ_Q_L
3V S3 WLAN FET
MOSFET TPCP8102
CHANNEL P-TYPE
RDS(ON) 20-30 MOHM @2.5V
LOADING 0.727 A (EDP)
727 MA PEAK
606 MA NOMINAL MAX
L3404
FERR-120-OHM-3A
PP3V3_WLAN
PP3V3_WLAN_F
XW3452
PP3V3_WLAN_R
CRITICAL
Q3450
TPCP8102
23V1K-SM
PP3V3_S3
PCIE_AP_R2D_P
PCIE_AP_R2D_N
C3431
C3430
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
C3422 0.1uF
C3421 0.1uF
C3420 10UF
C3450 0.1UF
C3451 0.033UF
R3450 33K
R3451 10K
P3V3WLAN_SS
PM_WLAN_EN_L
516S0582
CRITICAL
J3401
500913-0302
F-ST-SM
PCIE_AP_D2R_P
PCIE_AP_D2R_N
CRITICAL
L3401
90-OHM-100MA
DLP11S
AIRPORT
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
BLUETOOTH
L3403
90-OHM CRITICAL
DLP0NS
CONN_USB2_BT_P
CONN_USB2_BT_N
USB_BT_P
USB_BT_N
PP3V3_S3_BT_F
C3432 0.01UF
L3406
FERR-120-OHM-1.5A
0402-LF
PP3V3_S3
PCIE_WAKE_L
AP_RESET_CONN_L
RC (R3453 AND C3453)VALUE IS CHOSEN TO MEET THE 100 MS DELAY REQUIREMENT BETWEEN
3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET
PP3V3_WLAN_F
R3453 110K
U3402
74LVC1G17
SOT353-1
TC7SZ08AFEAPE
SOT665
U3401
WLAN_SMIT_BUF
AP_RESET_L
C3453 1UF
R3454 62K NOSTUFF
WLAN_SMIT_RC
R3455 1
WLAN_SMIT_DISCHRG
Q3401
SSM6N15FEAPE
PM_WLAN_EN_L
518S0767
CRITICAL
J3402
819Q-3506-K281
F-RT-SM
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
275 mA peak
206 mA nominal max
L3408
FERR-120-OHM-1.5A
PP5V_S3
C3452 0.1uF
ALS
CAMERA
CRITICAL
L3407
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
SYNC MASTER=K18 COMMS
SYNC DATE=06/15/2009
PAGE TITLE
X16/ALS/CAMERA CONNECTOR
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 34 OF 132
SHEET 33 OF 101
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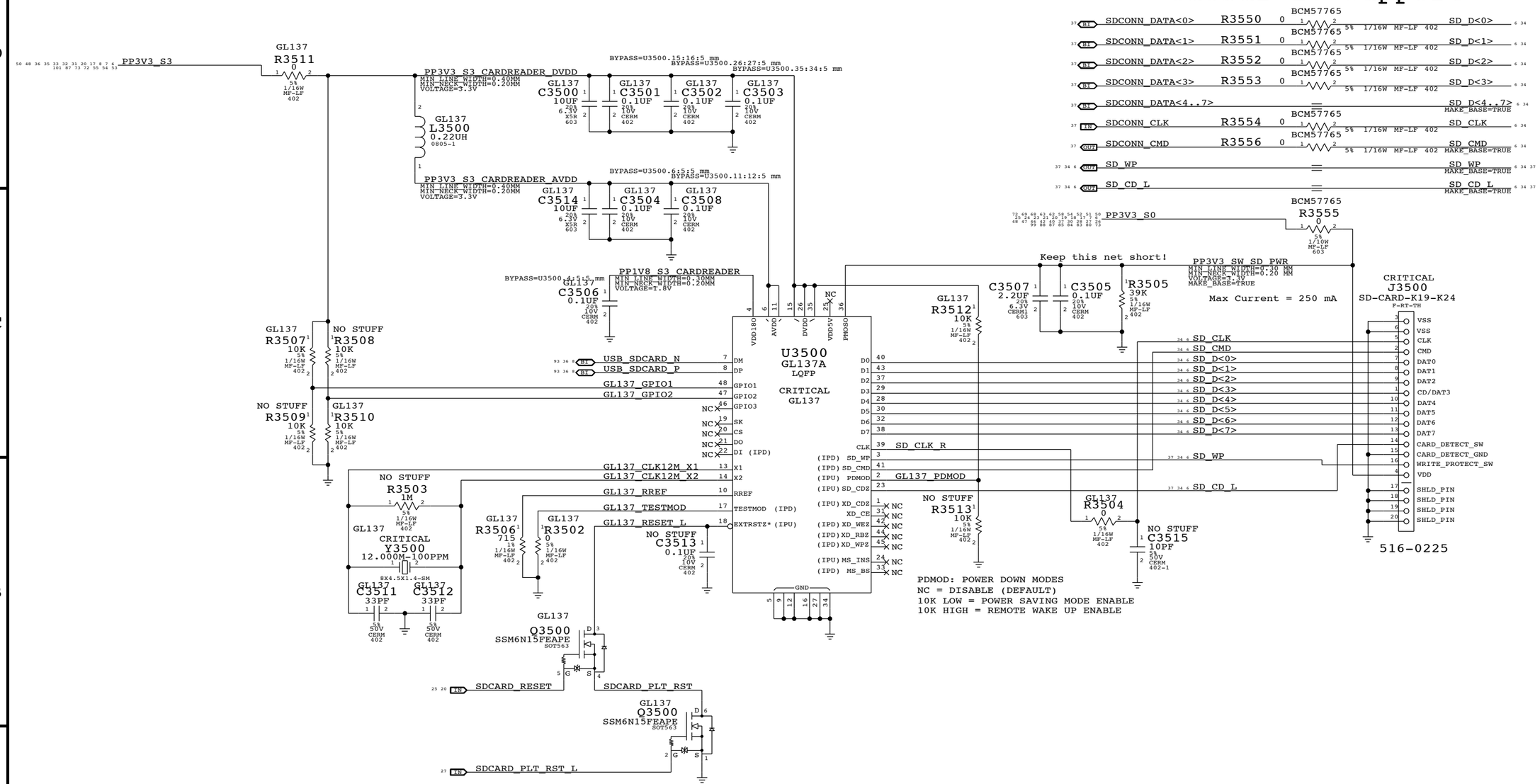
Caesar IV Support



SYNC MASTER=T27_REF SYNC DATE=08/26/2009

PAGE TITLE
SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 35 OF 132

SHEET 34 OF 101

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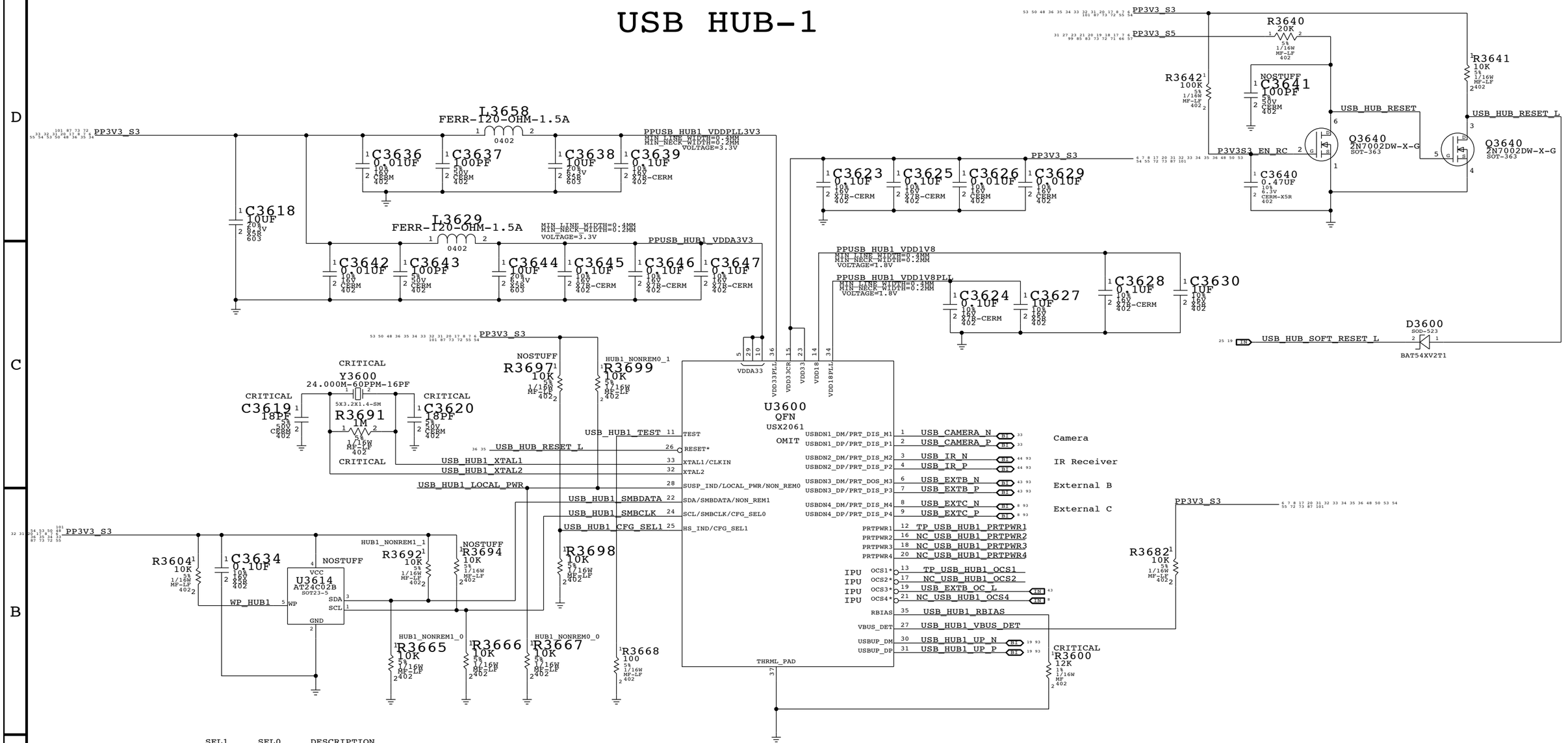
USB HUB-1



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC MASTER=K18 MLB SYNC DATE=10/07/2009

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 36 OF 132

SHEET: 35 OF 101

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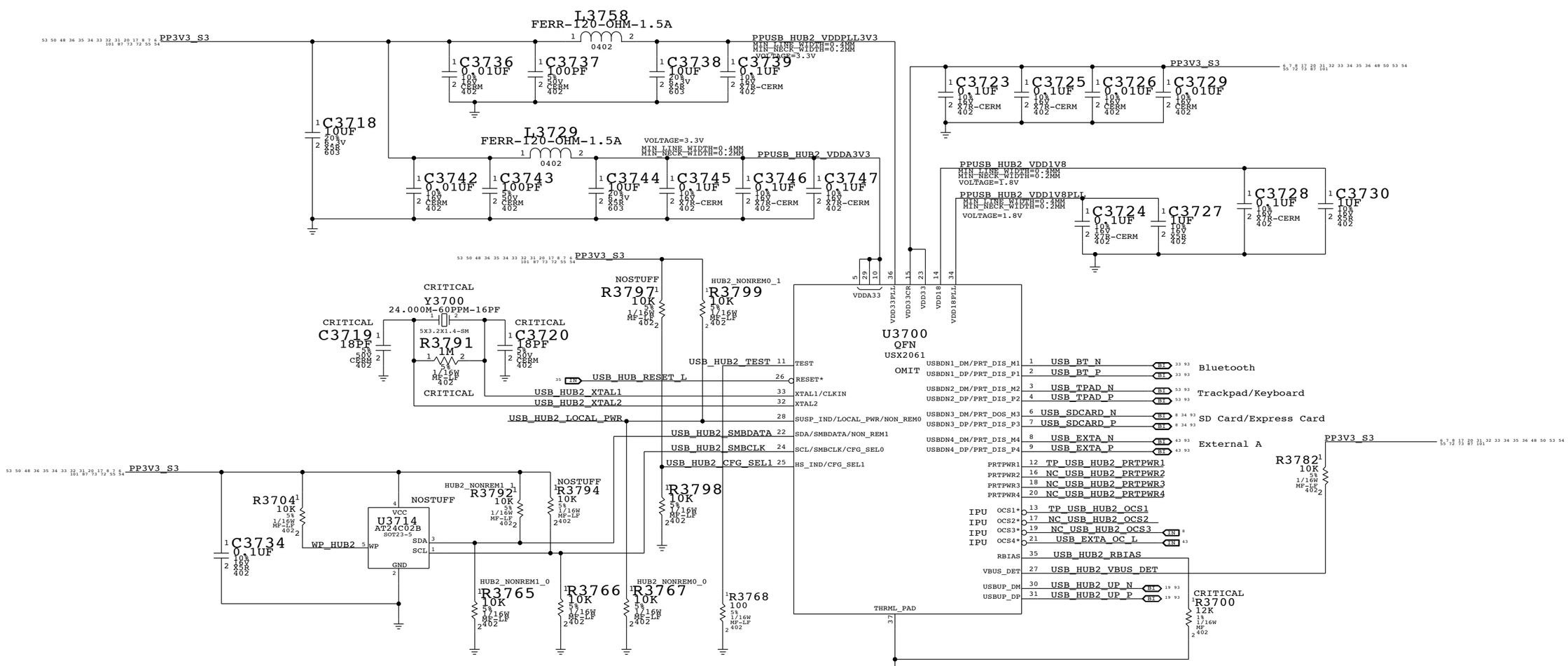
USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

SYNC MASTER=K23F SYNC DATE=10/06/2009

PAGE TITLE: USB HUB 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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PAGE: 37 OF 132

SHEET: 36 OF 101

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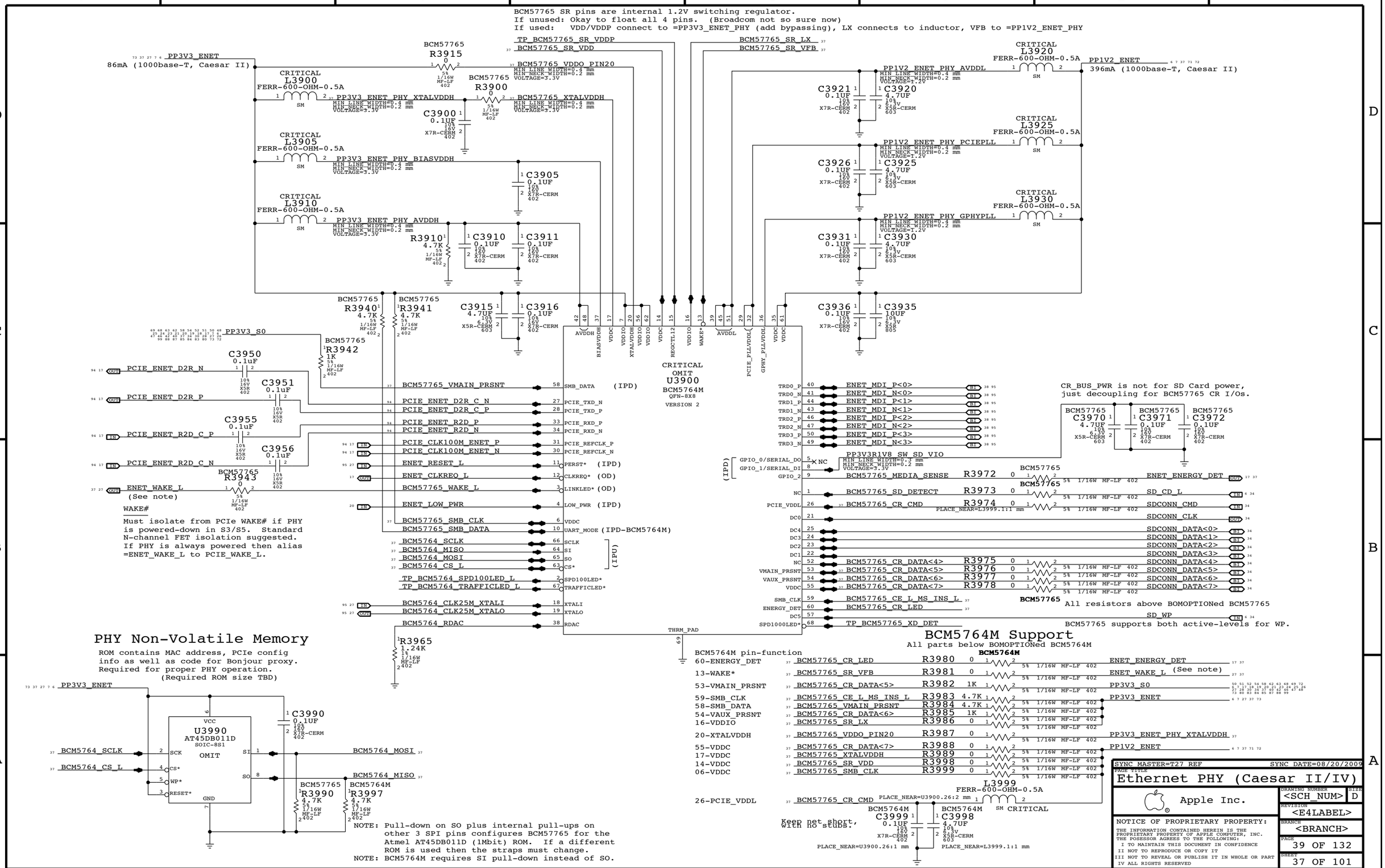
BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY
PP3V3_ENET
86mA (1000base-T, Caesar II)
CRITICAL L3900 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_XTALVDDH
BCM57765 R3915 0
BCM57765 R3900 0
BCM57765_VDDO_PIN20
BCM57765_XTALVDDH
C3900 0.1UF
CRITICAL L3905 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_BIASVDDH
C3905 0.1UF
CRITICAL L3910 FERR-600-OHM-0.5A
PP3V3_ENET_PHY_AVDDH
R3910 4.7K
C3910 0.1UF
C3911 0.1UF
C3915 4.7UF
C3916 0.1UF
TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_SR_LX
BCM57765_SR_VFB
CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET
396mA (1000base-T, Caesar II)
PP1V2_ENET_PHY_AVDDL
C3921 0.1UF
C3920 4.7UF
CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF
C3925 4.7UF
CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF
C3930 4.7UF
C3936 0.1UF
C3935 10UF
BCM57765 R3940 4.7K
BCM57765 R3941 4.7K
PP3V3_S0
BCM57765 R3942 1K
C3950 0.1uF
C3951 0.1uF
C3955 0.1uF
C3956 0.1uF
BCM57765 R3943 0
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
ENET_WAKE_L
(See note)
WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.
CRITICAL OMIT U3900 BCM5764M QFN-8X8 VERSION 2
BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC
SMB_DATA (IPD)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
(IPD)
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC
THRM_PAD
R3965 1.24K
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.
BCM57765 C3970 4.7UF
BCM57765 C3971 0.1UF
BCM57765 C3972 0.1UF
PP3V3R1V8_SW_SD_VIO
GPIO_0/SERIAL_DO
GPIO_1/SERIAL_DI
GPIO_2
BCM57765_MEDIA_SENSE R3972
ENET_ENERGY_DET
BCM57765_SD_DETECT R3973
SD_CD_L
BCM57765_CR_CMD R3974
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
BCM57765_CR_DATA<4> R3975
BCM57765_CR_DATA<5> R3976
BCM57765_CR_DATA<6> R3977
BCM57765_CR_DATA<7> R3978
BCM57765_CE_L_MS_INS_L
BCM57765_CR_LED
TP_BCM57765_XD_DET
SD_WP
All resistors above BOMOPTIONed BCM57765
BCM57765 supports both active-levels for WP.
BCM5764M Support
All parts below BOMOPTIONed BCM5764M
BCM5764M pin-function
60-ENERGY_DET
13-WAKE*
53-VMAIN_PRSNT
59-SMB_CLK
58-SMB_DATA
54-VAUX_PRSNT
16-VDDIO
20-XTALVDDH
55-VDDC
17-VDDC
14-VDDC
06-VDDC
26-PCIE_VDDL
BCM57765_CR_LED R3980
BCM57765_SR_VFB R3981
BCM57765_CR_DATA<5> R3982 1K
BCM57765_CE_L_MS_INS_L R3983 4.7K
BCM57765_VMAIN_PRSNT R3984 4.7K
BCM57765_CR_DATA<6> R3985 1K
BCM57765_SR_LX R3986
BCM57765_VDDO_PIN20 R3987
BCM57765_CR_DATA<7> R3988
BCM57765_XTALVDDH R3989
BCM57765_SR_VDD R3998
BCM57765_SMB_CLK R3999
ENET_ENERGY_DET
ENET_WAKE_L (See note)
PP3V3_S0
PP3V3_ENET
PP3V3_ENET_PHY_XTALVDDH
PP1V2_ENET
L3999 FERR-600-OHM-0.5A
BCM57765_CR_CMD
BCM5764M C3999 0.1UF
BCM5764M C3998 4.7UF
Keep net short, with no stubs.
PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)
U3990 AT45DB011D SOIC-8S1 OMIT
C3990 0.1UF
BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO
BCM57765 R3990 4.7K
BCM5764M R3997 4.7K
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.
SYNC MASTER=T27 REF
SYNC DATE=08/20/2009
PAGE TITLE
Ethernet PHY (Caesar II/IV)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 39 OF 132
SHEET 37 OF 101
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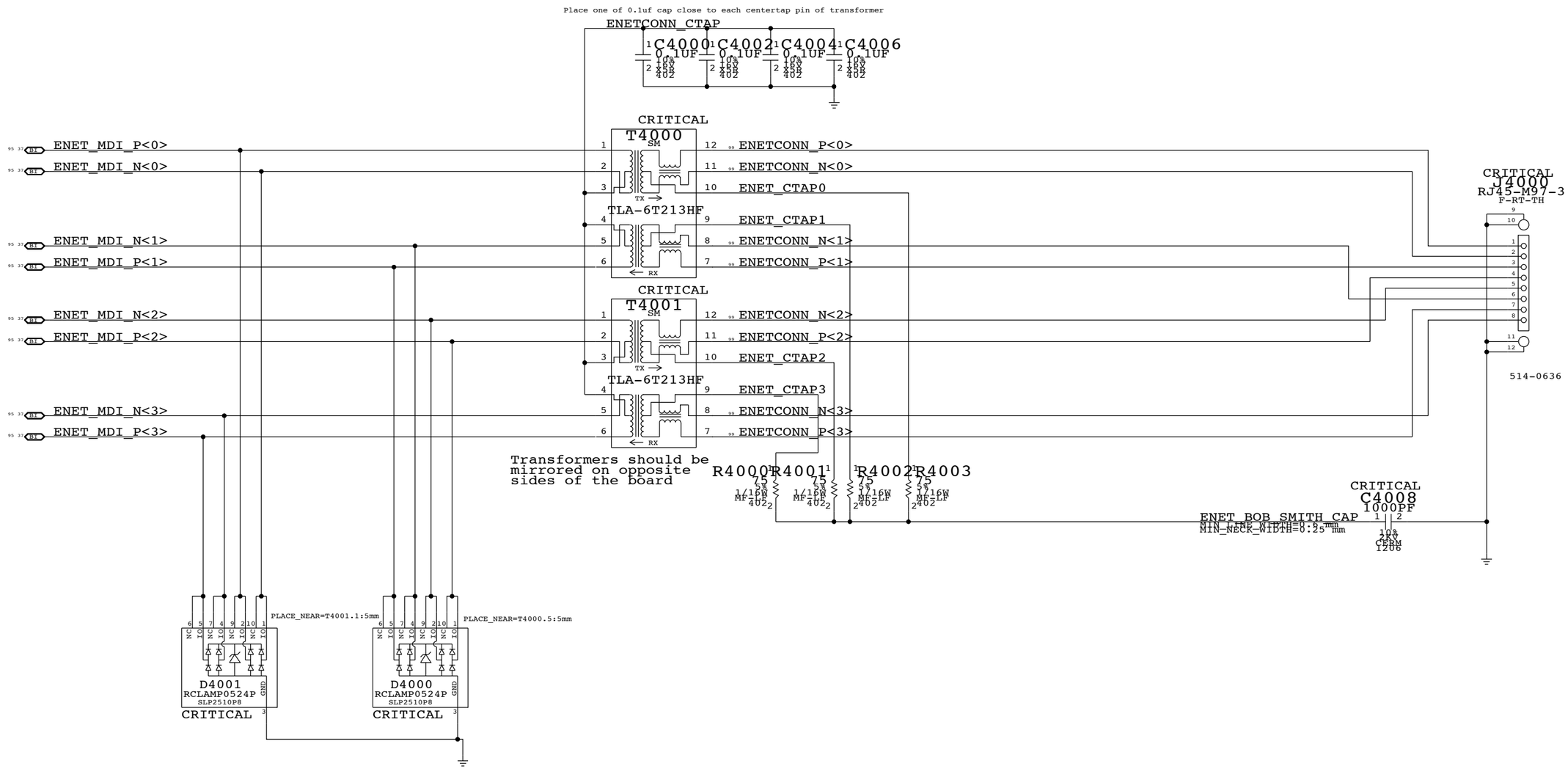
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
Ethernet Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 40 OF 132

SHEET 38 OF 101

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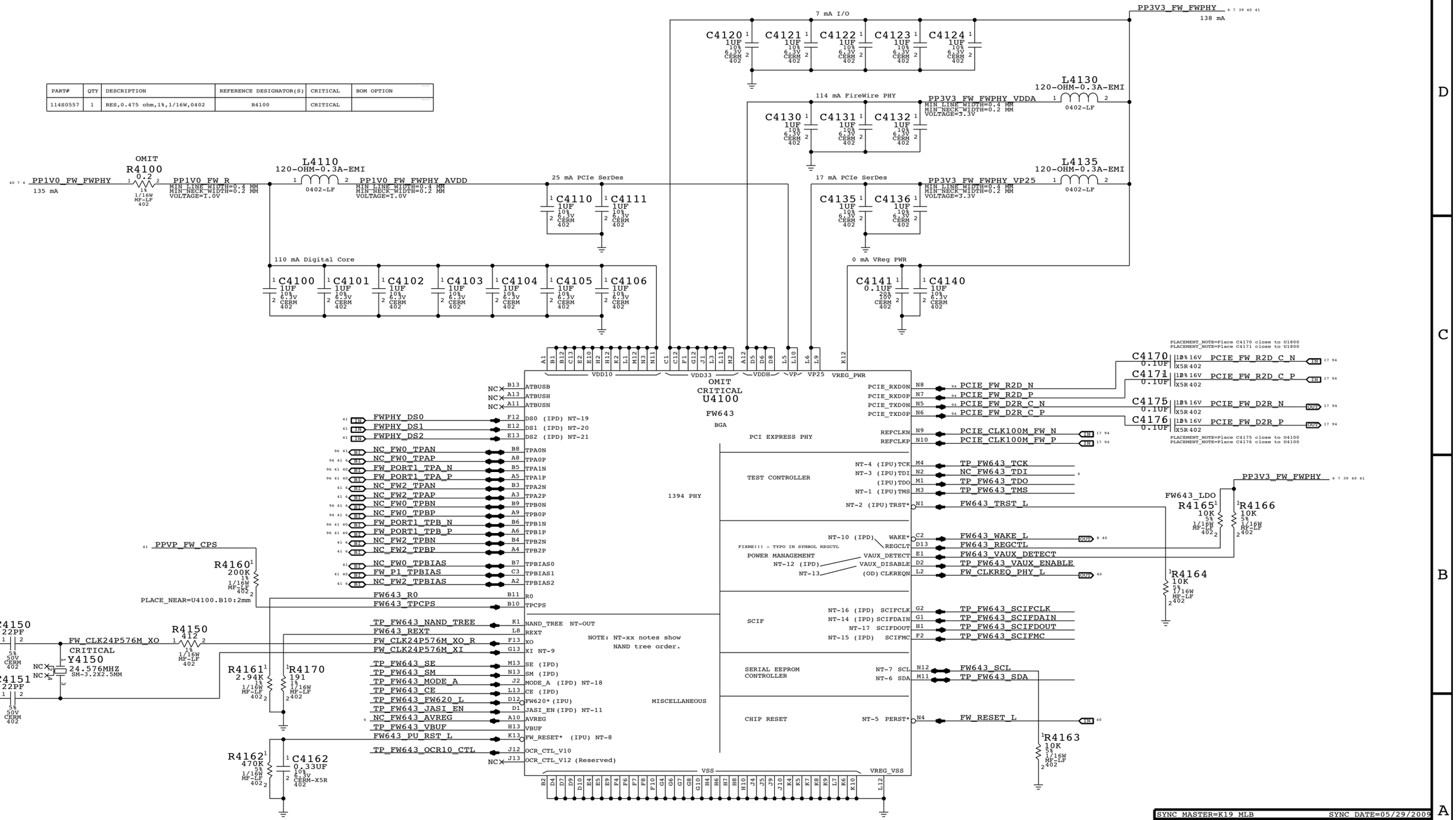
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	



SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 41 OF 132

SHEET 39 OF 101

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Page Notes

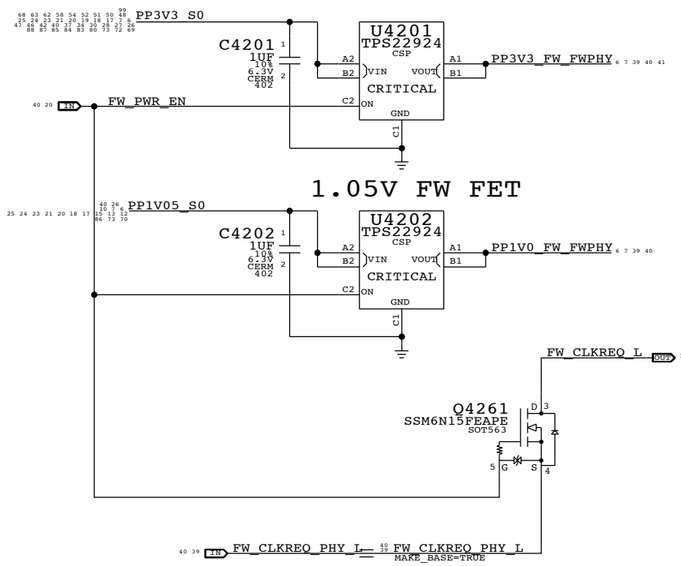
Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

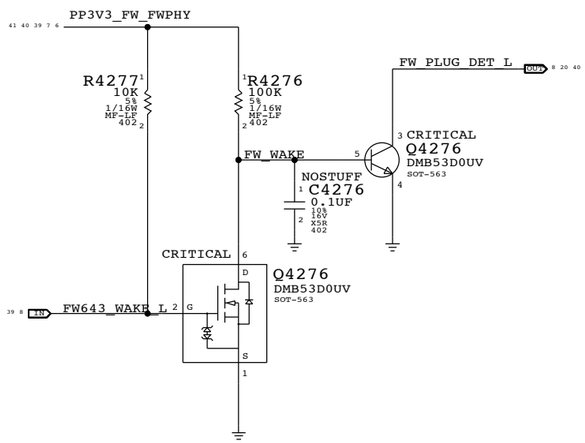
Signal aliases required by this page:
(NONE)

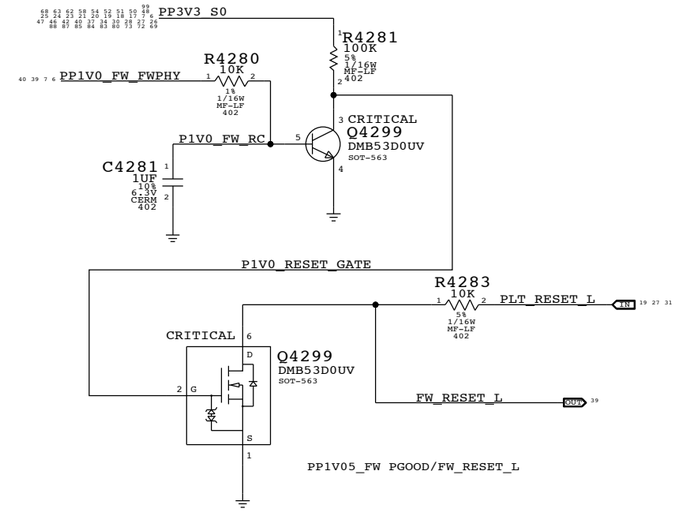
BOM options provided by this page:

3.3V FW FET

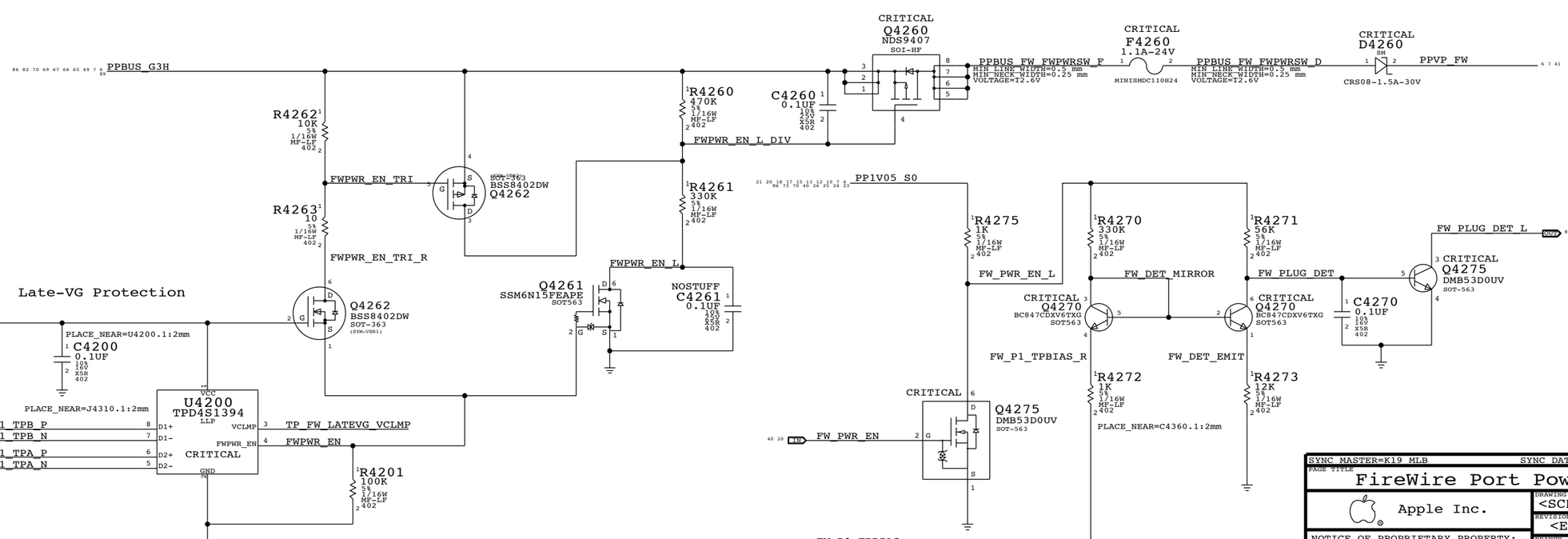
I(max) = 1.7A (85C)



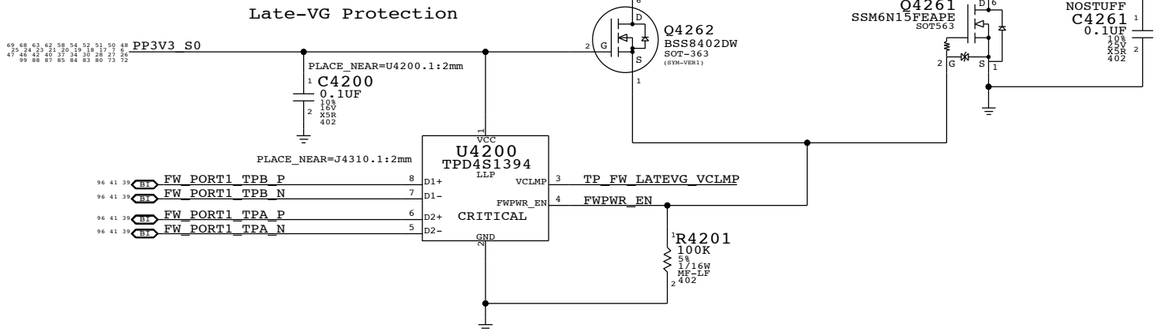




FireWire Port Power Switch



Late-VG Protection



SYNC MASTER=K19_MLB	SYNC DATE=05/29/2009
PAGE TITLE: FireWire Port Power	
Apple Inc.	DRAWING NUMBER: <SCH NUM> SIZE: D
	REVISION: <E4LABEL>
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	PAGE: 42 OF 132
	SHEET: 40 OF 101

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

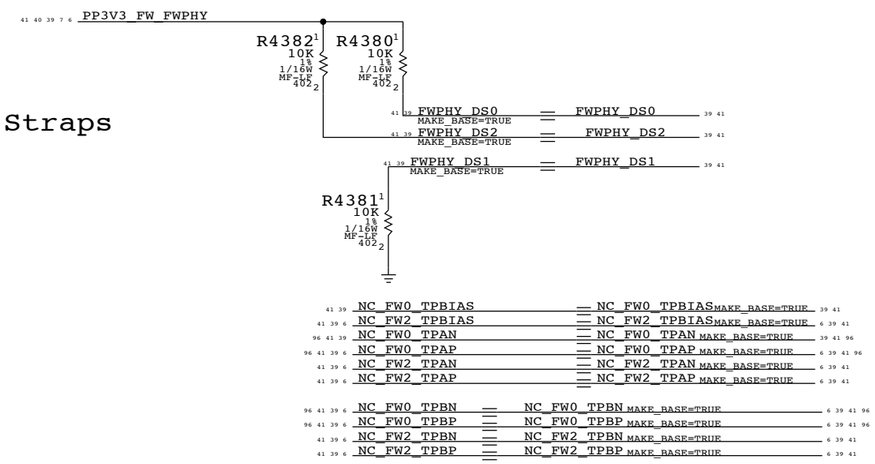
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

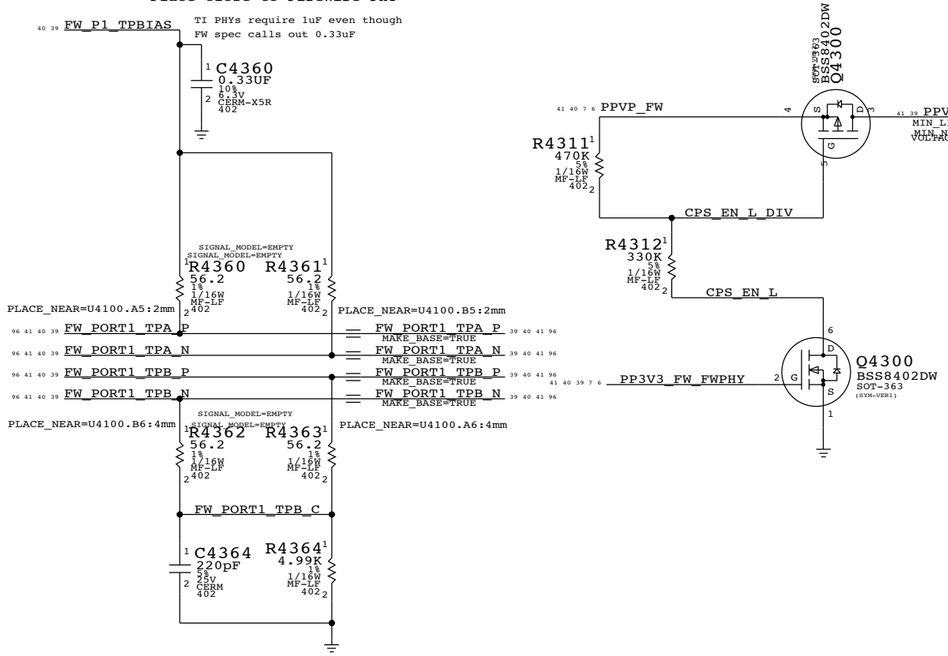
- 1-port Portable Power Class (0)

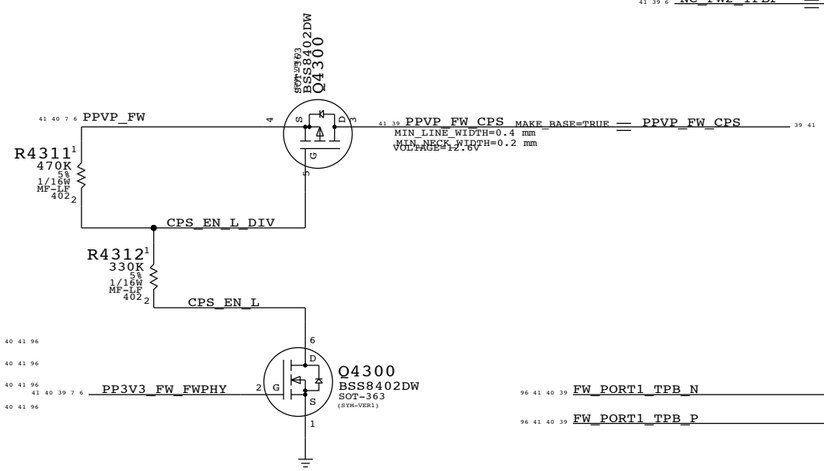
- Port "1" Bilingual (1394B)

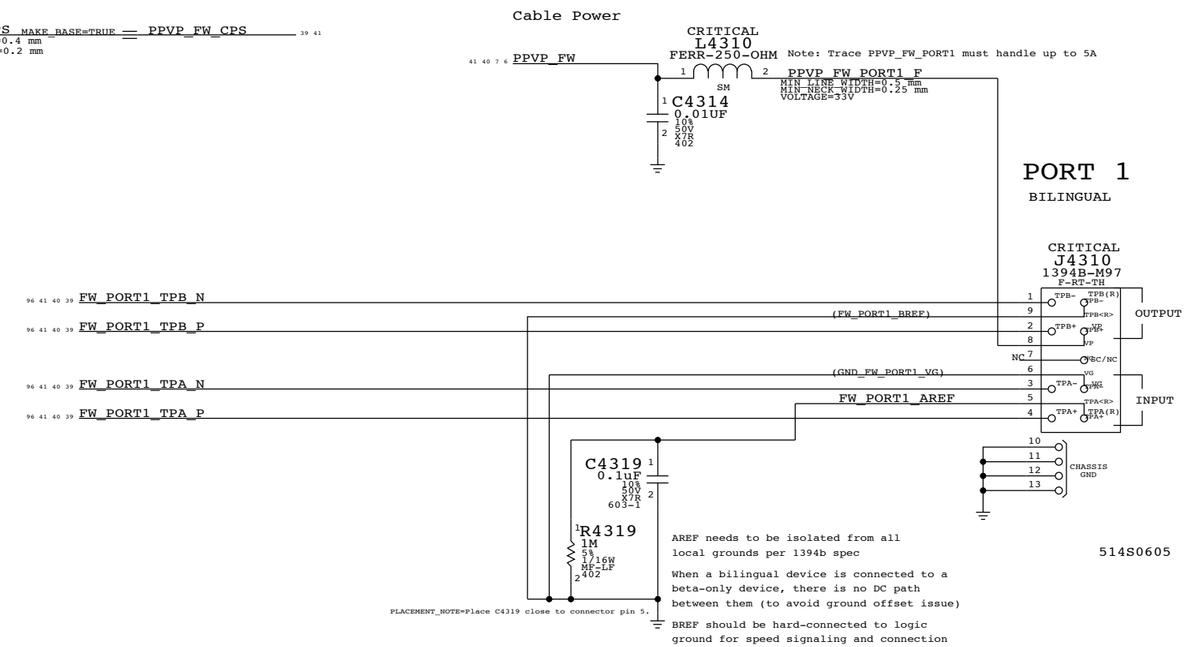


Termination

Place close to FireWire PHY







SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE
FireWire Ports

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 43 OF 132
SHEET 41 OF 101

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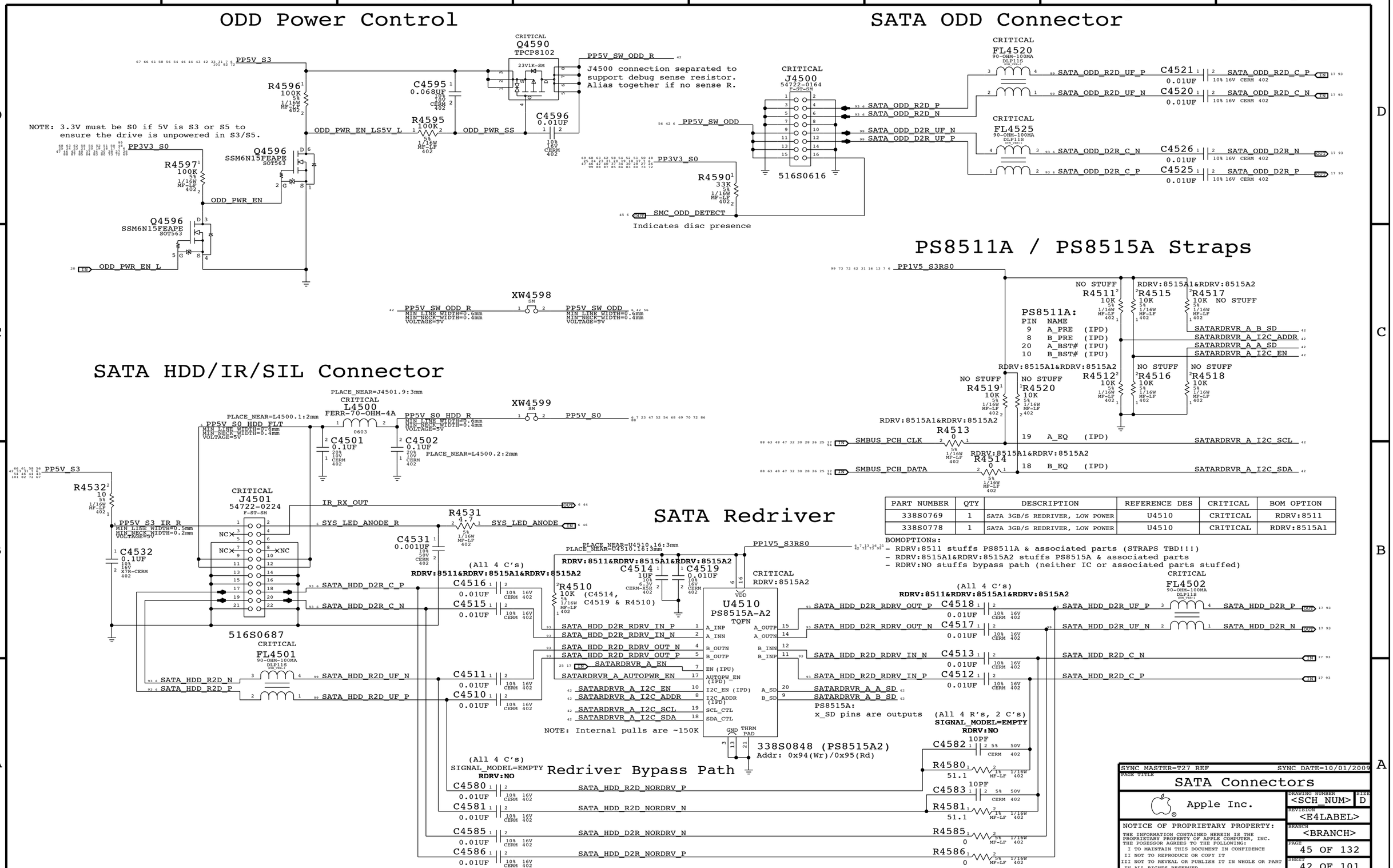
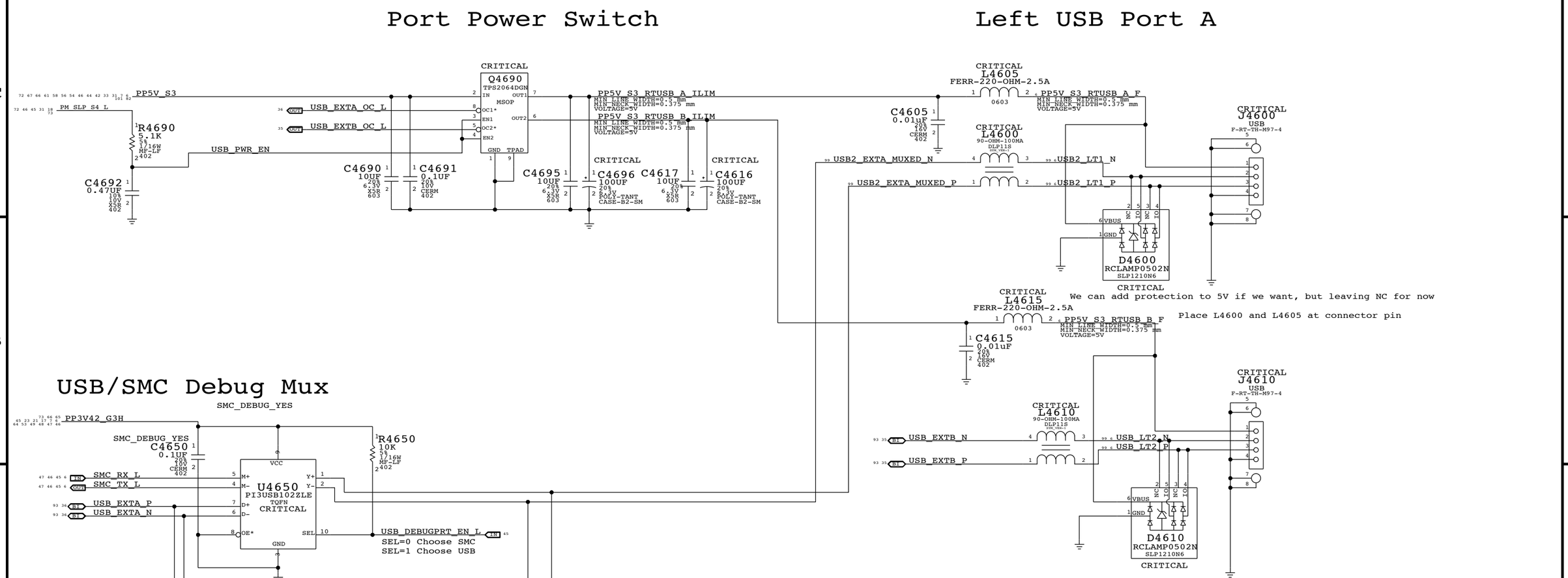


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8515A1



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 46 OF 132

SHEET 43 OF 101

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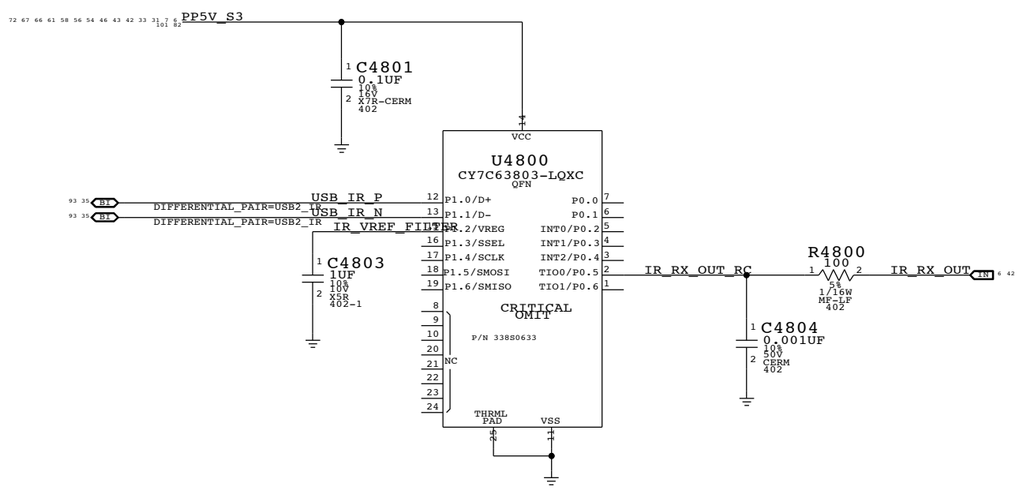
IR SUPPORT



SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 48 OF 132

SHEET 44 OF 101

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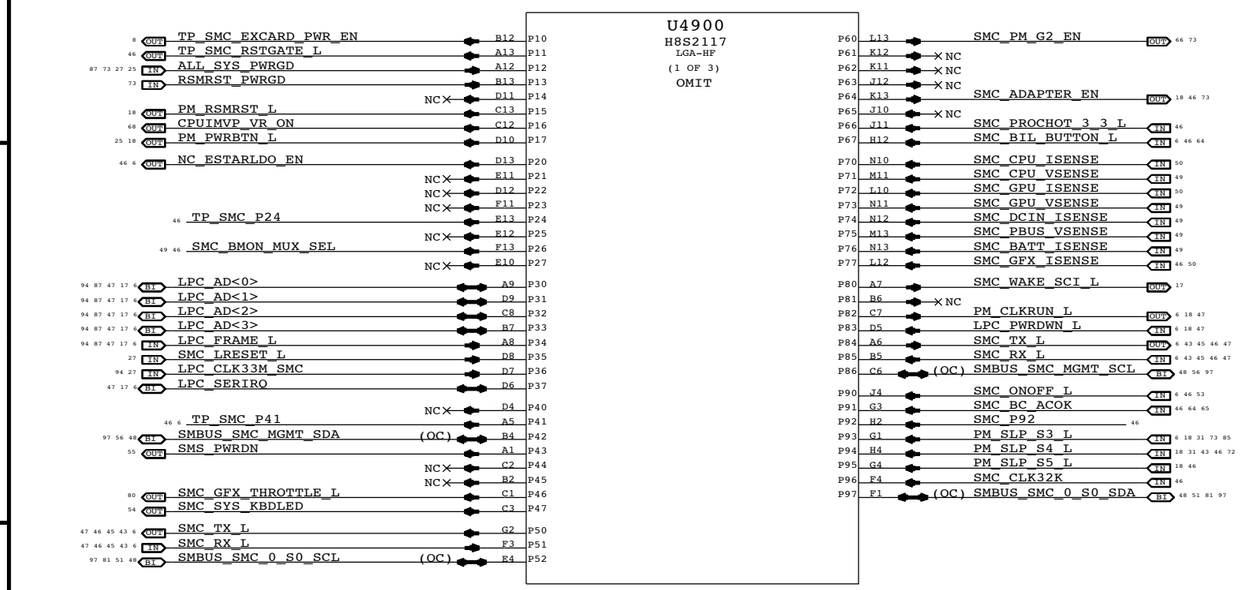
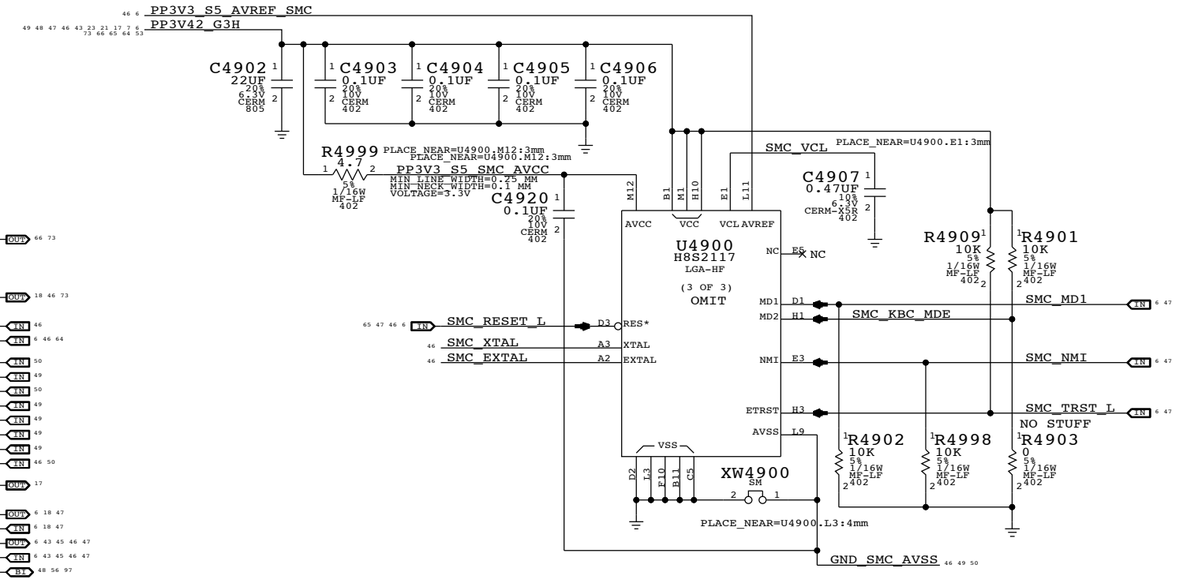
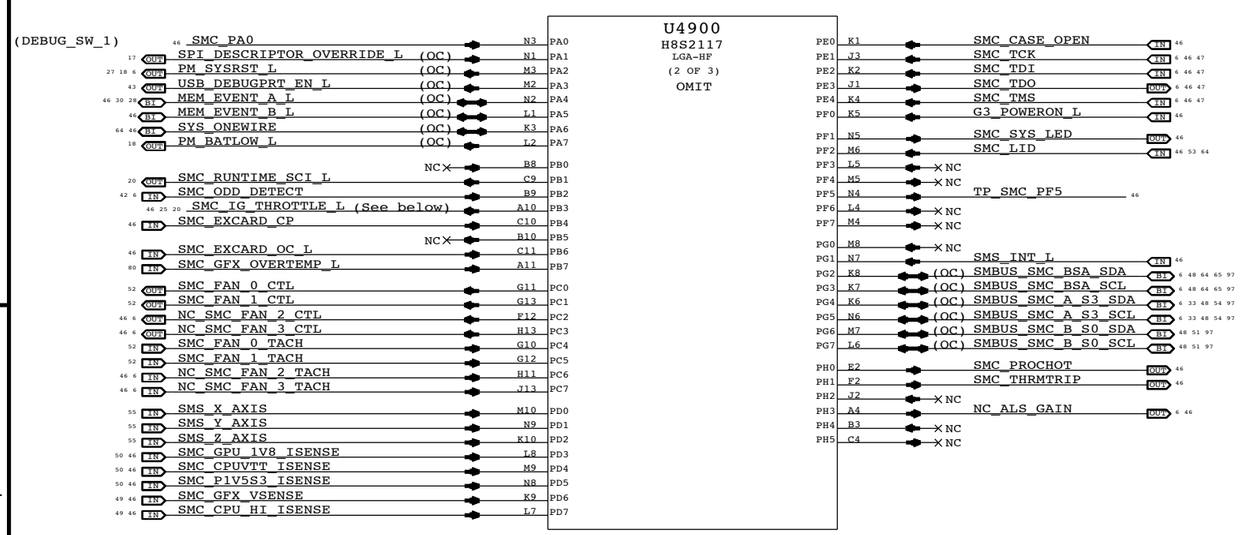
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 49 OF 132
SHEET 45 OF 101

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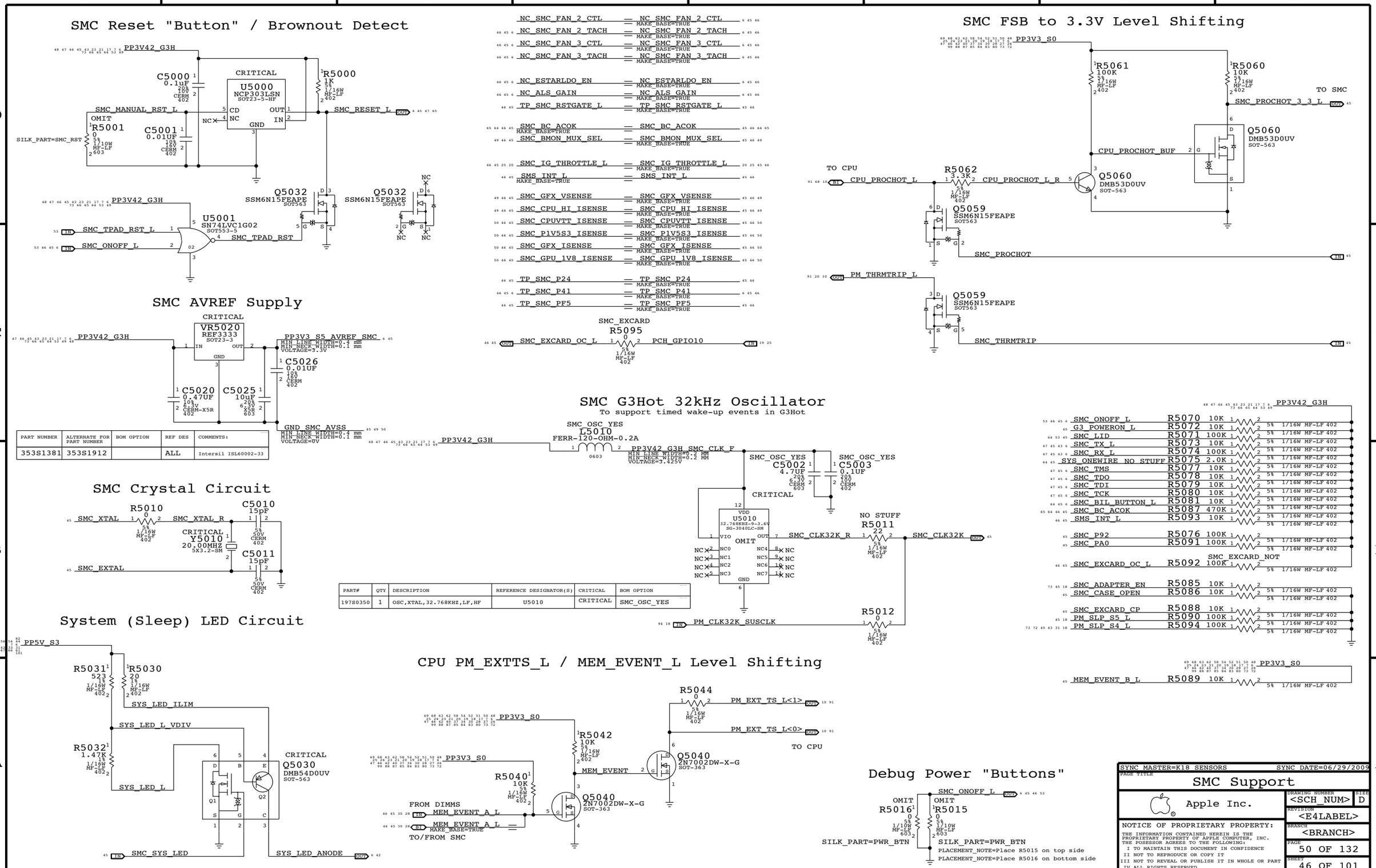
SMC Reset "Button" / Brownout Detect
PP3V42_G3H
C5000 0.1uF 10% 16V CERM 402
CRITICAL
U5000 NCP303LSN SOT23-5-HF
R5000 1K 5% 1/16W MF-LF 402
SMC_MANUAL_RST_L
SMC_RESET_L
OMIT
R5001 0 5% 1/10W MF-LF 603
SILK_PART=SMC_RST
C5001 0.01UF 10% 16V CERM 402
Q5032 SSM6N15FEAPE SOT563
U5001 SN74LVC1G02 SOT553-5
SMC_TPAD_RST_L
SMC_ONOFF_L
SMC_TPAD_RST
NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH
NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH
NC_ESTARLDO_EN
NC_ALS_GAIN
TP_SMC_RSTGATE_L
SMC_BC_ACOK
SMC_BMON_MUX_SEL
SMC_IG_THROTTLE_L
SMS_INT_L
SMC_GFX_VSENSE
SMC_CPU_HI_ISENSE
SMC_CPUVTT_ISENSE
SMC_P1V5S3_ISENSE
SMC_GFX_ISENSE
SMC_GPU_1V8_ISENSE
TP_SMC_P24
TP_SMC_P41
TP_SMC_PF5
SMC_EXCARD
R5095 0 5% 1/16W MF-LF 402
SMC_EXCARD_OC_L
PCH_GPIO10
SMC FSB to 3.3V Level Shifting
PP3V3_S0
R5061 100K 5% 1/16W MF-LF 402
R5060 10K 5% 1/16W MF-LF 402
TO SMC
SMC_PROCHOT_3_3_L
Q5060 DMB53D0UV SOT-563
CPU_PROCHOT_BUF
TO CPU
CPU_PROCHOT_L
R5062 3.3K 5% 1/16W MF-LF 402
CPU_PROCHOT_L_R
Q5059 SSM6N15FEAPE SOT563
SMC_PROCHOT
PM_THRMTRIP_L
SMC_THRMTRIP
SMC AVREF Supply
CRITICAL
VR5020 REF3333 SOT23-3
PP3V42_G3H
PP3V3_S5_AVREF_SMC
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=3.3V
C5026 0.01UF 10% 16V CERM 402
C5020 0.47UF 10% 6.3V CERM-X5R 402
C5025 10uF 20% 6.3V X5R 603
GND_SMC_AVSS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=0V
SMC G3Hot 32kHz Oscillator
To support timed wake-up events in G3Hot
SMC_OSC_YES
L5010 FERR-120-OHM-0.2A
PP3V42_G3H_SMC_CLK_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.425V
C5002 4.7UF 20% 6.3V CERM 603
C5003 0.1UF 20% 10V CERM 402
U5010 32.768KHZ-9-3.6V SG-3040LC-SM
OMIT
SMC_CLK32K_R
NO STUFF
R5011 22 5% 1/16W MF-LF 402
SMC_CLK32K
R5012 0 5% 1/16W MF-LF 402
PM_CLK32K_SUSCLK
PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION
197S0350 | 1 | OSC,XTAL,32.768KHZ,LF,HF | U5010 | CRITICAL | SMC_OSC_YES
PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:
353S1381 | 353S1912 | | ALL | Intersil ISL60002-33
SMC Crystal Circuit
R5010 0 5% 1/16W MF-LF 402
SMC_XTAL
SMC_XTAL_R
C5010 15pF 5% 50V CERM 402
CRITICAL
Y5010 20.00MHZ 5X3.2-SM
C5011 15pF 5% 50V CERM 402
SMC_EXTAL
System (Sleep) LED Circuit
PP5V_S3
R5031 523 1% 1/16W MF-LF 402
R5030 20 1% 1/16W MF-LF 402
SYS_LED_ILIM
SYS_LED_L_VDIV
R5032 1.47K 1% 1/16W MF-LF 402
SYS_LED_L
CRITICAL
Q5030 DMB54D0UV SOT-563
SMC_SYS_LED
SYS_LED_ANODE
CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting
R5044 0 5% 1/16W MF-LF 402
PM_EXT_TS_L<1>
PM_EXT_TS_L<0>
TO CPU
R5042 10K 5% 1/16W MF-LF 402
MEM_EVENT
Q5040 2N7002DW-X-G SOT-363
R5040 10K 5% 1/16W MF-LF 402
FROM DIMMS
MEM_EVENT_A_L
TO/FROM SMC
Debug Power "Buttons"
SMC_ONOFF_L
OMIT
R5016 0 5% 1/10W MF-LF 603
R5015 0 5% 1/10W MF-LF 603
SILK_PART=PWR_BTN
PLACEMENT_NOTE=Place R5015 on top side
PLACEMENT_NOTE=Place R5016 on bottom side
SMC_ONOFF_L R5070 10K 5% 1/16W MF-LF 402
G3_POWERON_L R5072 10K 5% 1/16W MF-LF 402
SMC_LID R5071 100K 5% 1/16W MF-LF 402
SMC_TX_L R5073 10K 5% 1/16W MF-LF 402
SMC_RX_L R5074 100K 5% 1/16W MF-LF 402
SYS_ONEWIRE_NO_STUFF R5075 2.0K 5% 1/16W MF-LF 402
SMC_TMS R5077 10K 5% 1/16W MF-LF 402
SMC_TDO R5078 10K 5% 1/16W MF-LF 402
SMC_TDI R5079 10K 5% 1/16W MF-LF 402
SMC_TCK R5080 10K 5% 1/16W MF-LF 402
SMC_BIL_BUTTON_L R5081 10K 5% 1/16W MF-LF 402
SMC_BC_ACOK R5087 470K 5% 1/16W MF-LF 402
SMS_INT_L R5093 10K 5% 1/16W MF-LF 402
SMC_P92 R5076 100K 5% 1/16W MF-LF 402
SMC_PA0 R5091 100K 5% 1/16W MF-LF 402
SMC_EXCARD_NOT
SMC_EXCARD_OC_L R5092 100K 5% 1/16W MF-LF 402
SMC_ADAPTER_EN R5085 10K 5% 1/16W MF-LF 402
SMC_CASE_OPEN R5086 100K 5% 1/16W MF-LF 402
SMC_EXCARD_CP R5088 10K 5% 1/16W MF-LF 402
PM_SLP_S5_L R5090 100K 5% 1/16W MF-LF 402
PM_SLP_S4_L R5094 100K 5% 1/16W MF-LF 402
MEM_EVENT_B_L R5089 10K 5% 1/16W MF-LF 402
SYNC MASTER=K18 SENSORS
SYNC DATE=06/29/2009
PAGE TITLE
SMC Support
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 50 OF 132
SHEET 46 OF 101
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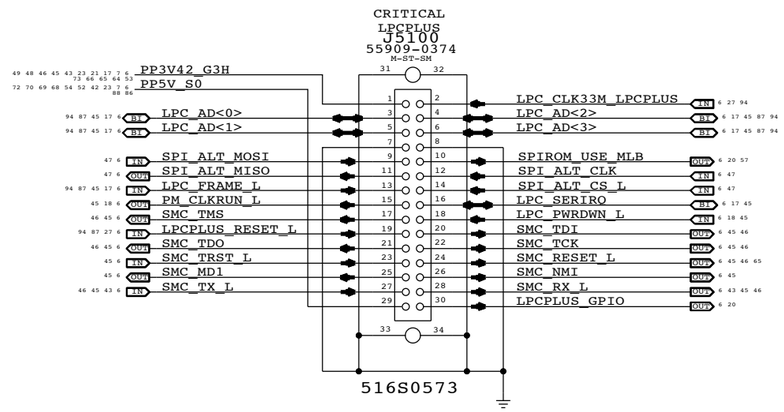
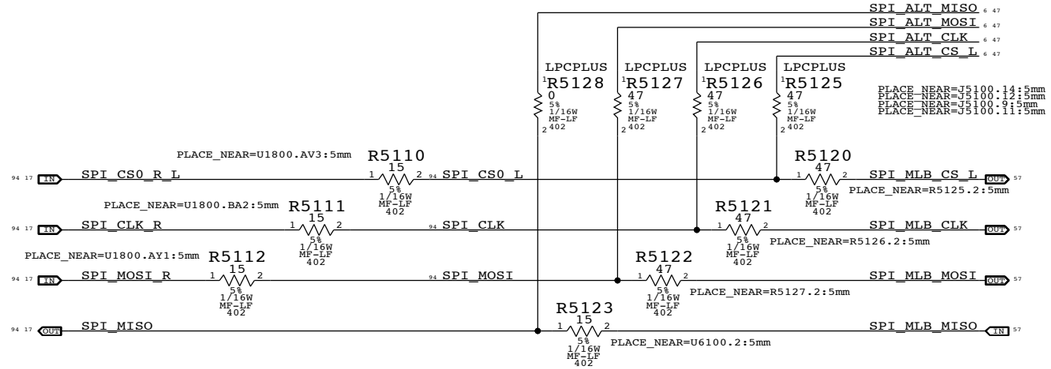
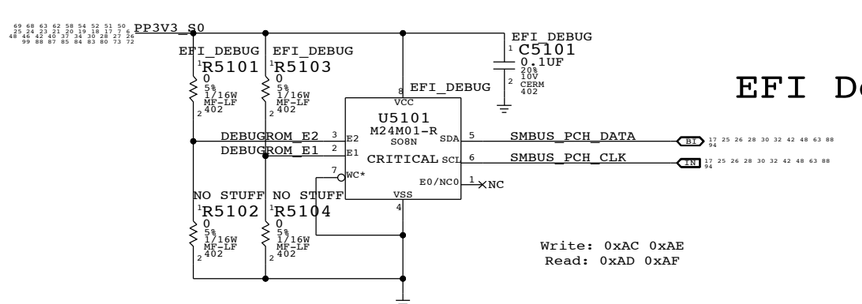
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC MASTER=K17 MLB SYNC DATE=06/23/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 51 OF 132

SHEET 47 OF 101

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402 — R5201 1K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)
SMBUS_PCH_CLK (MAKE_BASE=TRUE)
SMBUS_PCH_DATA (MAKE_BASE=TRUE)

VRef DACs
U2900
(Write: 0x98 Read: 0x99)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

Margin Control
U2901
(Write: 0x30 Read: 0x31)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

EFI Debug Serial
U5101
(Write: 0xAC/AE Read: 0xAD/AF)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

XDP Connectors
J2600 & J2650
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

CK505 (Clock)
U2700
(Write: 0xD2 Read: 0xD3)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

Mikey
U6800
(Write: 0x72 Read: 0x73)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

HDD Redriver Control A
U4510
(Write: 0x94 Read: 0x95)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402 — R5211 8.2K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)
SML_PCH_0_CLK (MAKE_BASE=TRUE)
SML_PCH_0_DATA (MAKE_BASE=TRUE)

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF R5220 8.2K 5% 1/16W MF-LF 402 — NO STUFF R5221 8.2K 5% 1/16W MF-LF 402

R5223 0 5% 1/16W MF-LF 402

R5222 0 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(Write: 0x90 Read: 0x91)
SML_PCH_1_CLK (MAKE_BASE=TRUE)
SML_PCH_1_DATA (MAKE_BASE=TRUE)

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402 — R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
GT216: U8000
(Write: 0x9E Read: 0x9F)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402 — R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

Trackpad
J5800
(Write: 0x90 Read: 0x91)
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x72 Read: 0x73)
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402 — R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 1K 5% 1/16W MF-LF 402 — R5281 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

R5290 4.7K 5% 1/16W MF-LF 402 — R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA

SYNC MASTER=K18 SENSORS SYNC DATE=06/18/2009

PAGE TITLE
K18 SMBus Connections

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PAGE 52 OF 132
SHEET 48 OF 101

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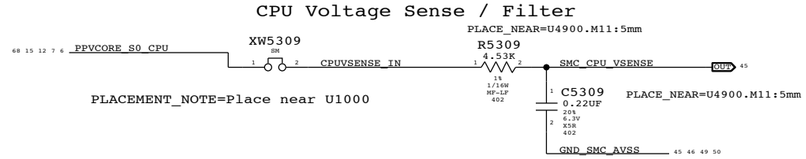
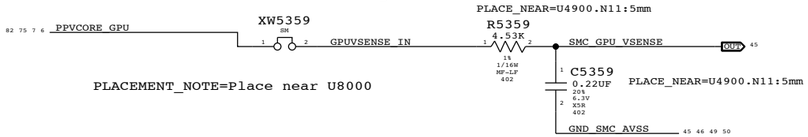
CPU Voltage Sense / Filter



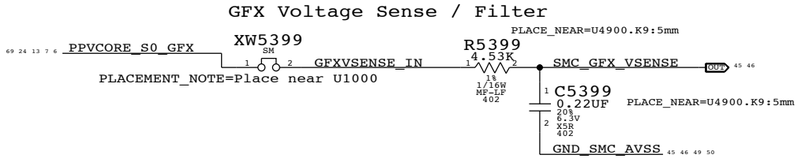
PLACEMENT_NOTE=Place near U1000

GPU Voltage Sense / Filter



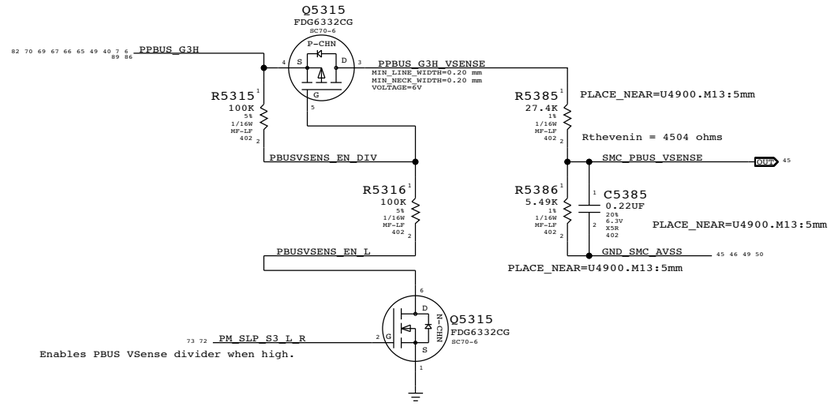
PLACEMENT_NOTE=Place near U8000

GFX Voltage Sense / Filter



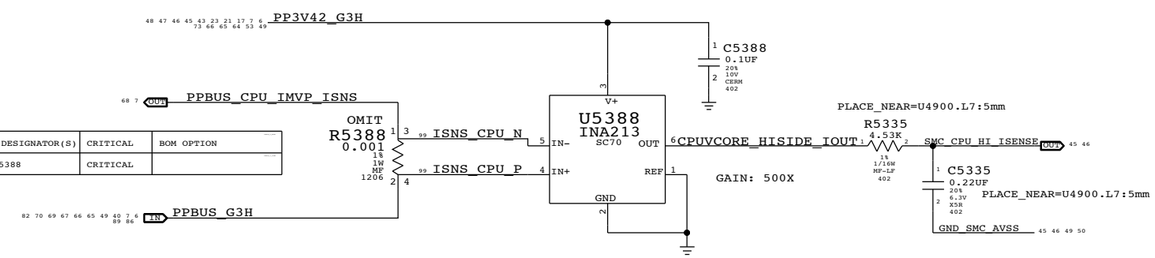
PLACEMENT_NOTE=Place near U1000

PBUS Voltage Sense & Filter



Enables PBUS VSense divider when high.

CPU VCore High Side Current Sensor

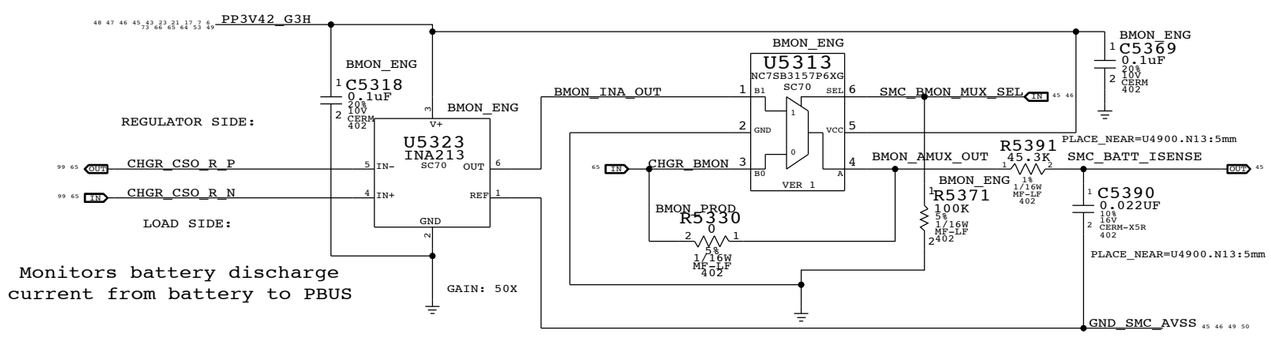


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
102S0858	1	RES,0.010 OHM,1%,1/2W,1206	R5388	CRITICAL	

GAIN: 500X

EDP for PPVIN_S5_CPU_IMVP_ISNS_R = 5.867 amps for K18.

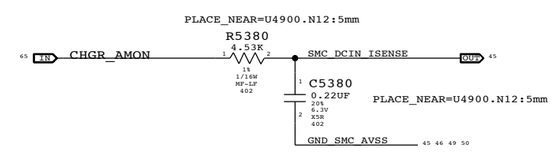
BMON Current Sense - Entire circuit must be near SMC (U4900)



Monitors battery discharge current from battery to PBUS

U5303 only senses current up to 6.6A

DCIN Current Sense Filter



SYNC MASTER=K18 SENSORS SYNC DATE=06/29/2009

PAGE TITLE
Current & Voltage Sensing

Apple Inc.

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PAGE 53 OF 132

SHEET 49 OF 101

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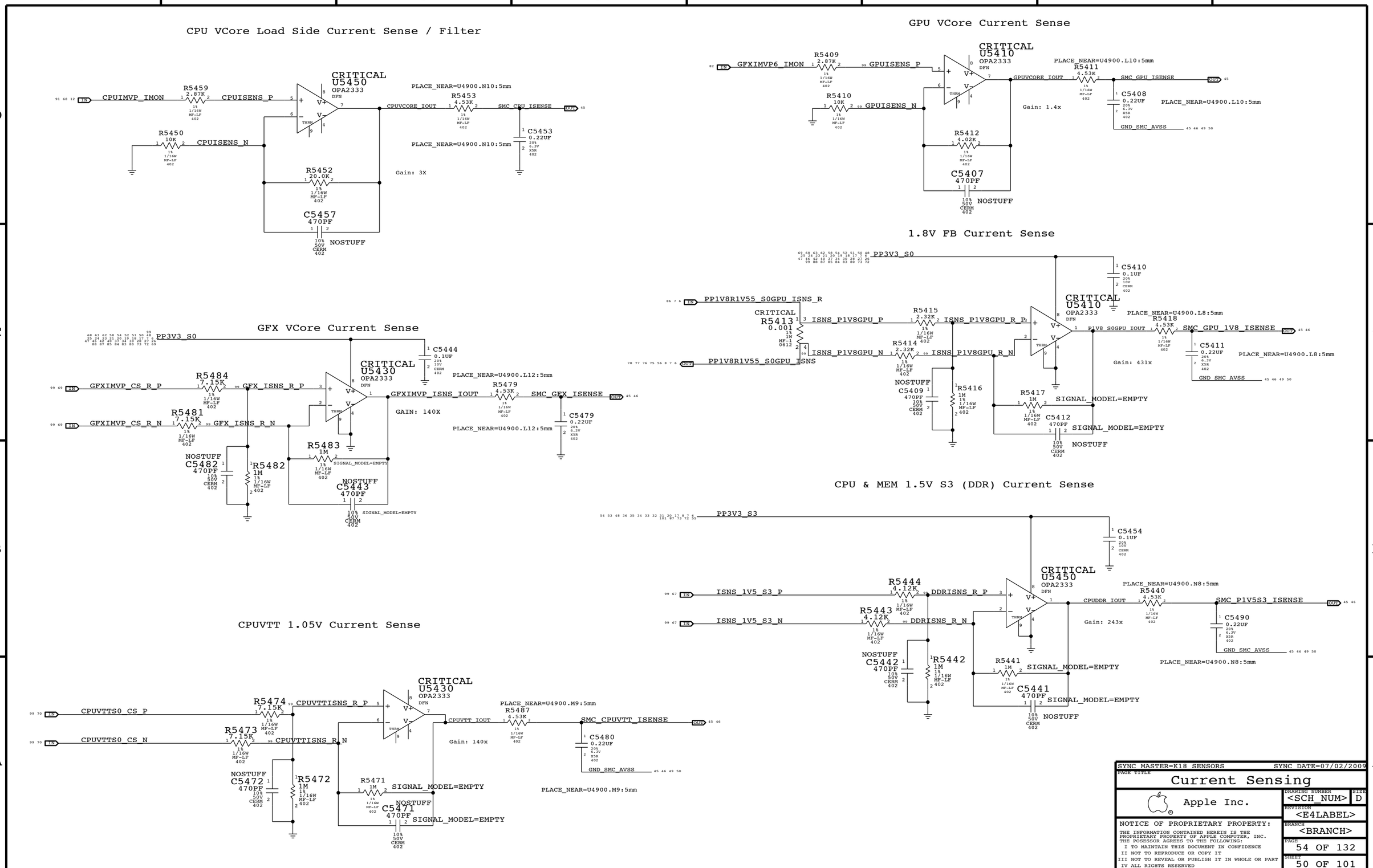

SYNC MASTER=K18 SENSORS SYNC DATE=07/02/2009

PAGE TITLE

Current Sensing

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PAGE 54 OF 132

SHEET 50 OF 101

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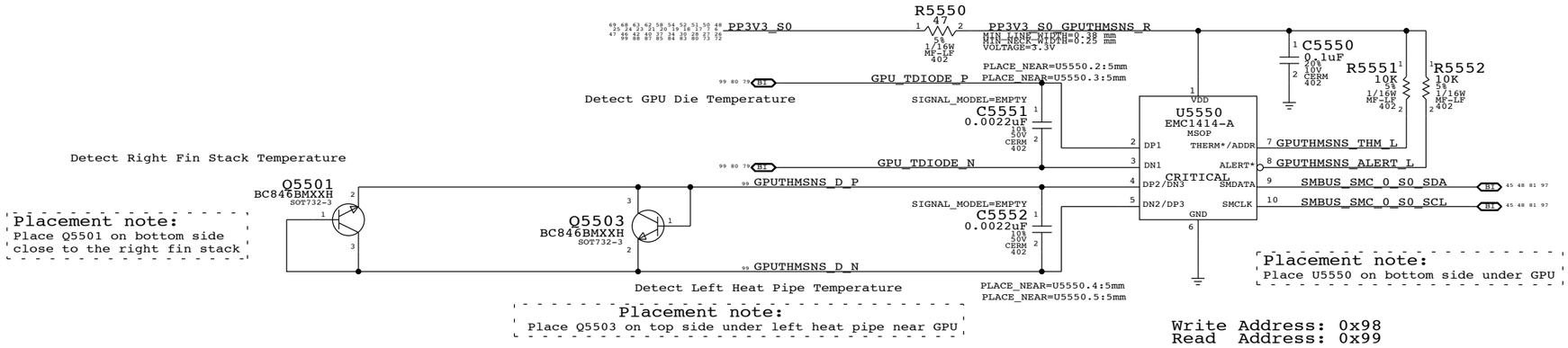
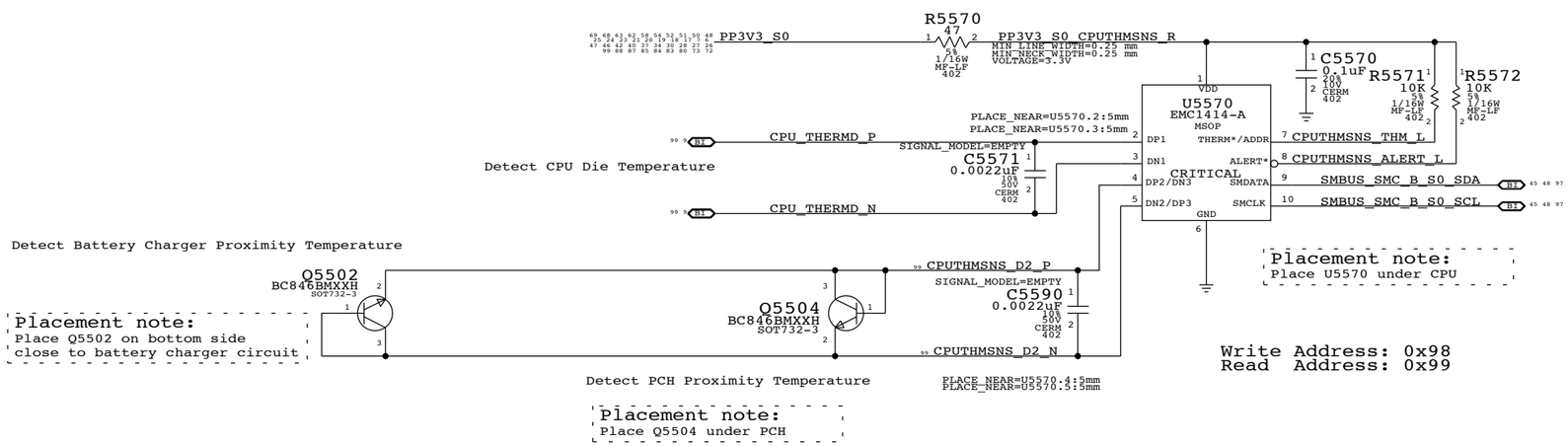
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

SYNC MASTER=K18 SENSORS SYNC DATE=06/18/2009

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	55 OF 132
SHEET	51 OF 101

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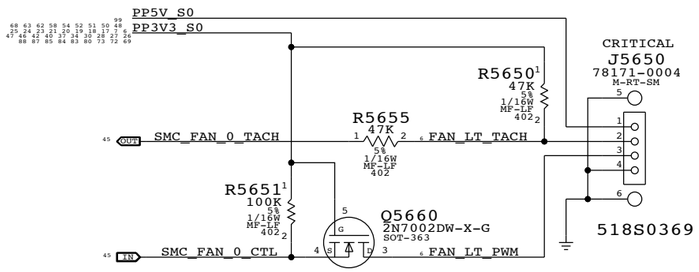
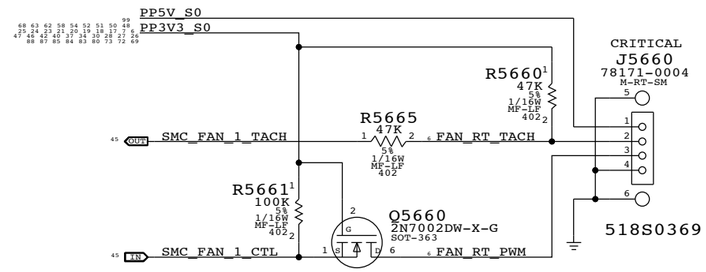
Left Fan



Right Fan



SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE

Fan Connectors

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PAGE 56 OF 132

SHEET 52 OF 101

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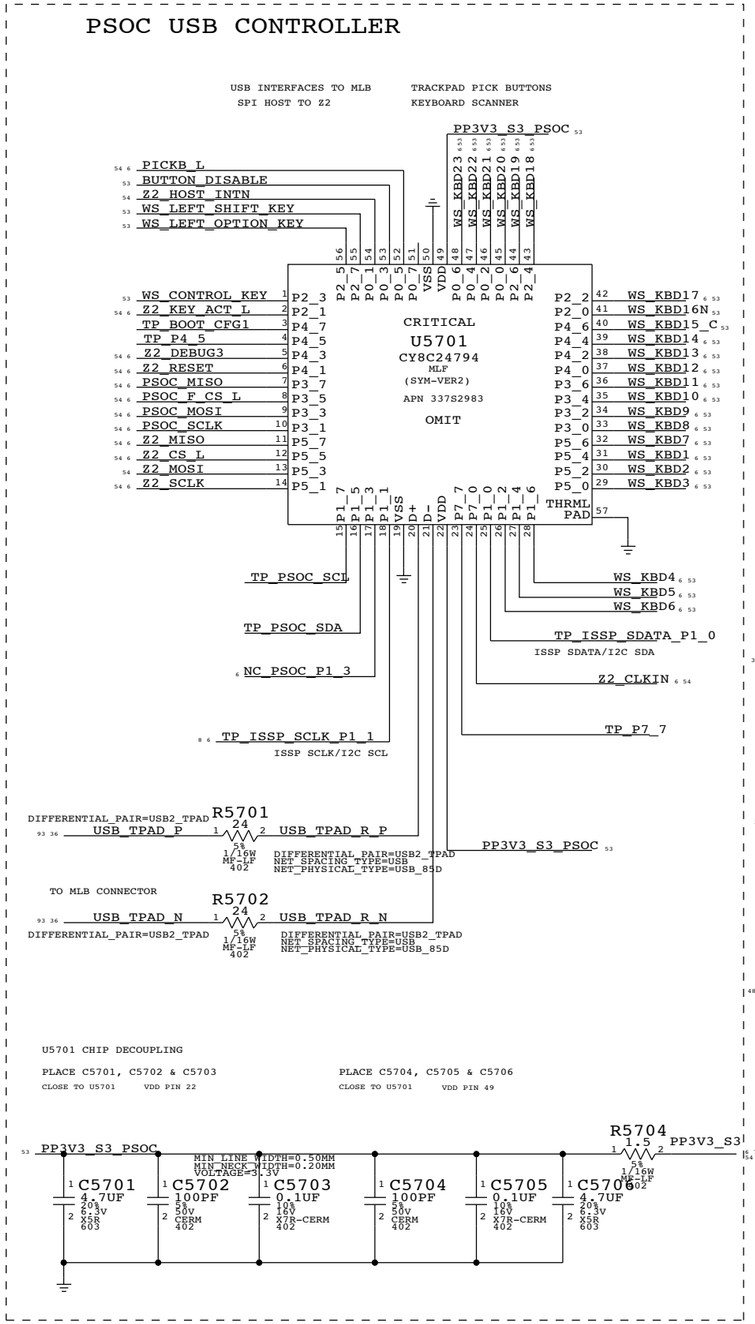
PSOC USB CONTROLLER



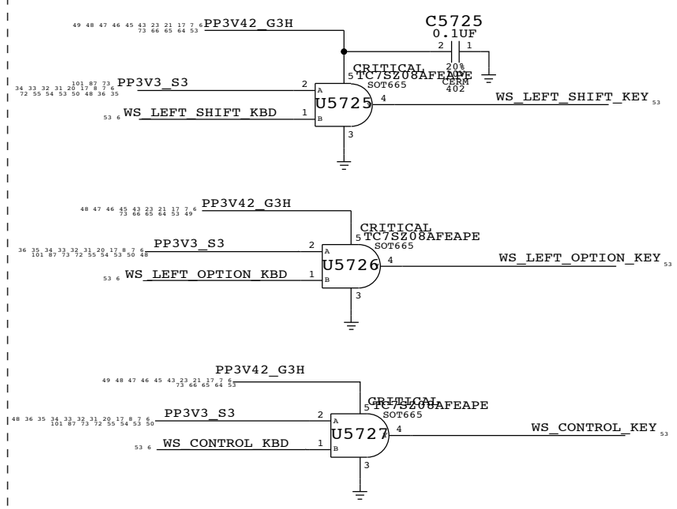
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

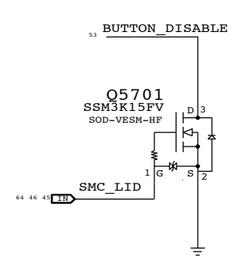
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



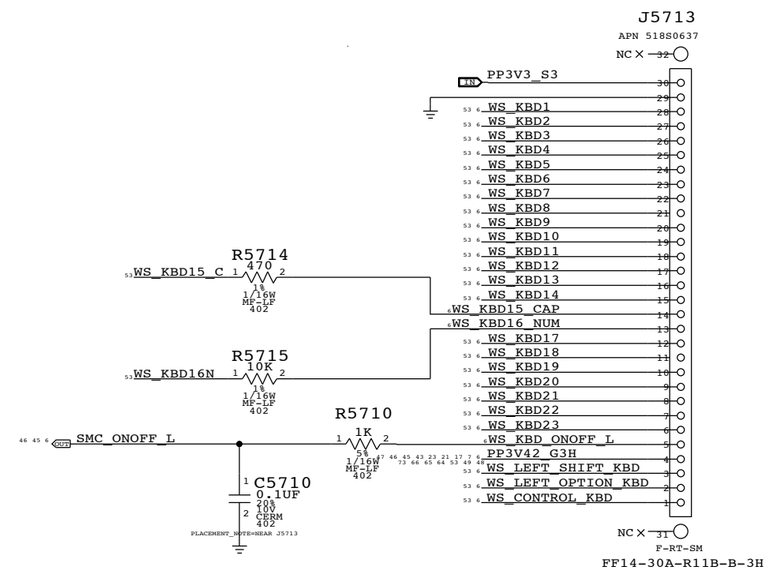
TPAD BUTTONS DISABLE



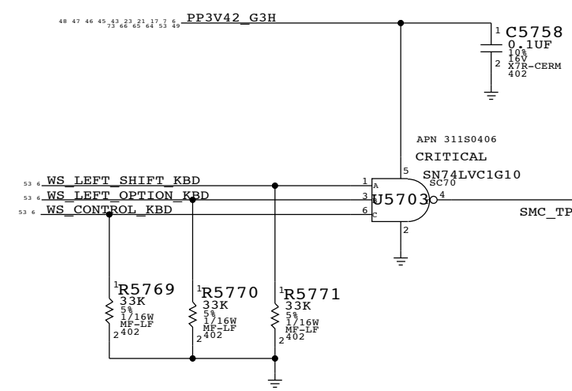
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE
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PAGE 57 OF 132
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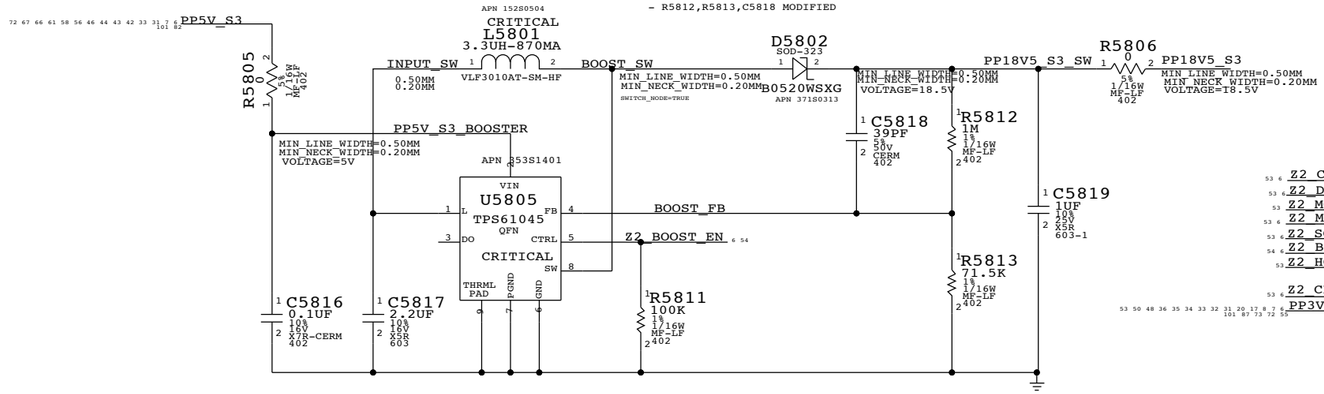
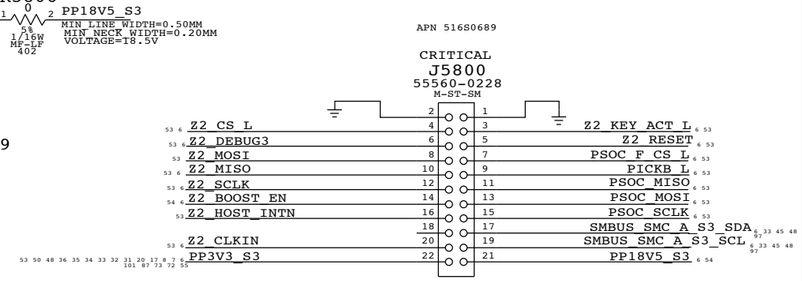
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



Keyboard LED Driver

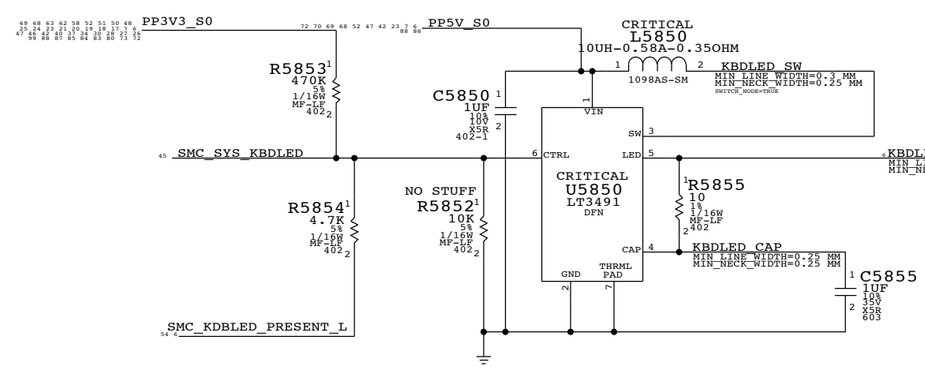
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

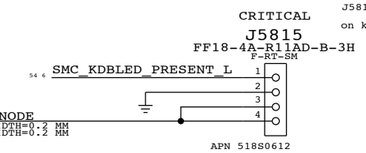
HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT



J5815 pin 1 is grounded on keyboard backlight flex



KBD BACKLIGHT CONNECTOR

SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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PAGE: 58 OF 132

SHEET: 54 OF 101

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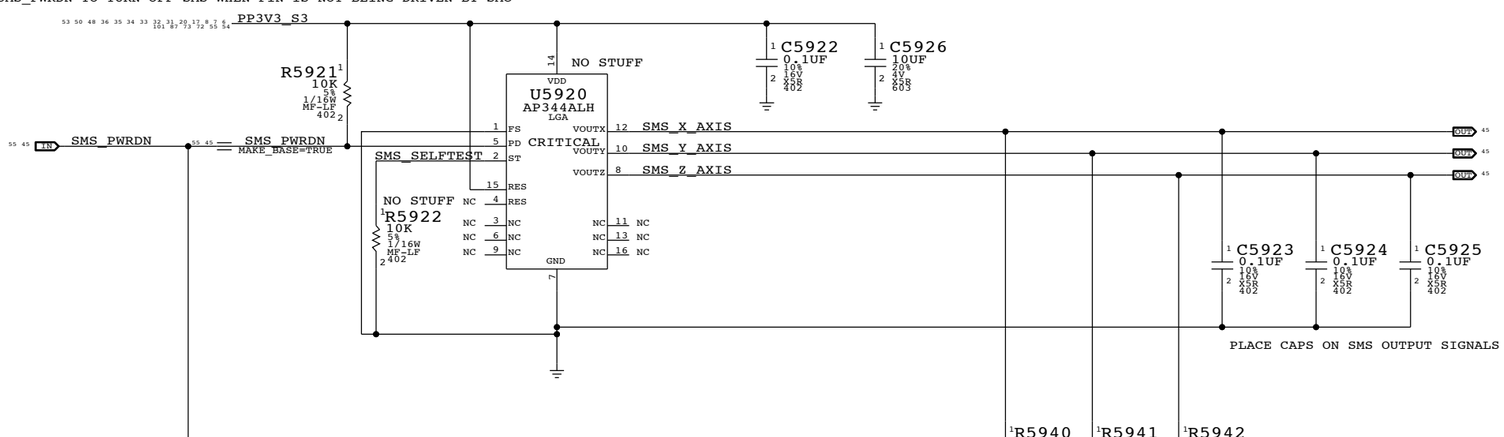
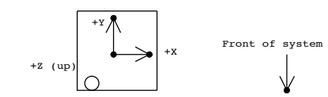
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

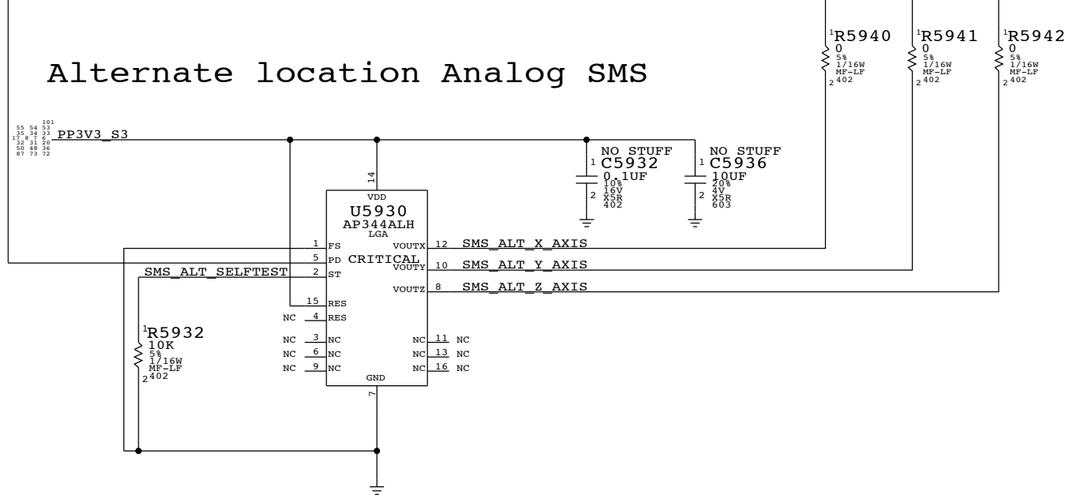


PLACE CAPS ON SMS OUTPUT SIGNALS CLOSE TO SMC

Desired orientation when placed on board top-side:

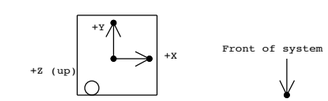


Circle indicates pin 1 location when placed in correct orientation



Alternate location Analog SMS

Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE
Sudden Motion Sensor (SMS)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 59 OF 132

SHEET 55 OF 101

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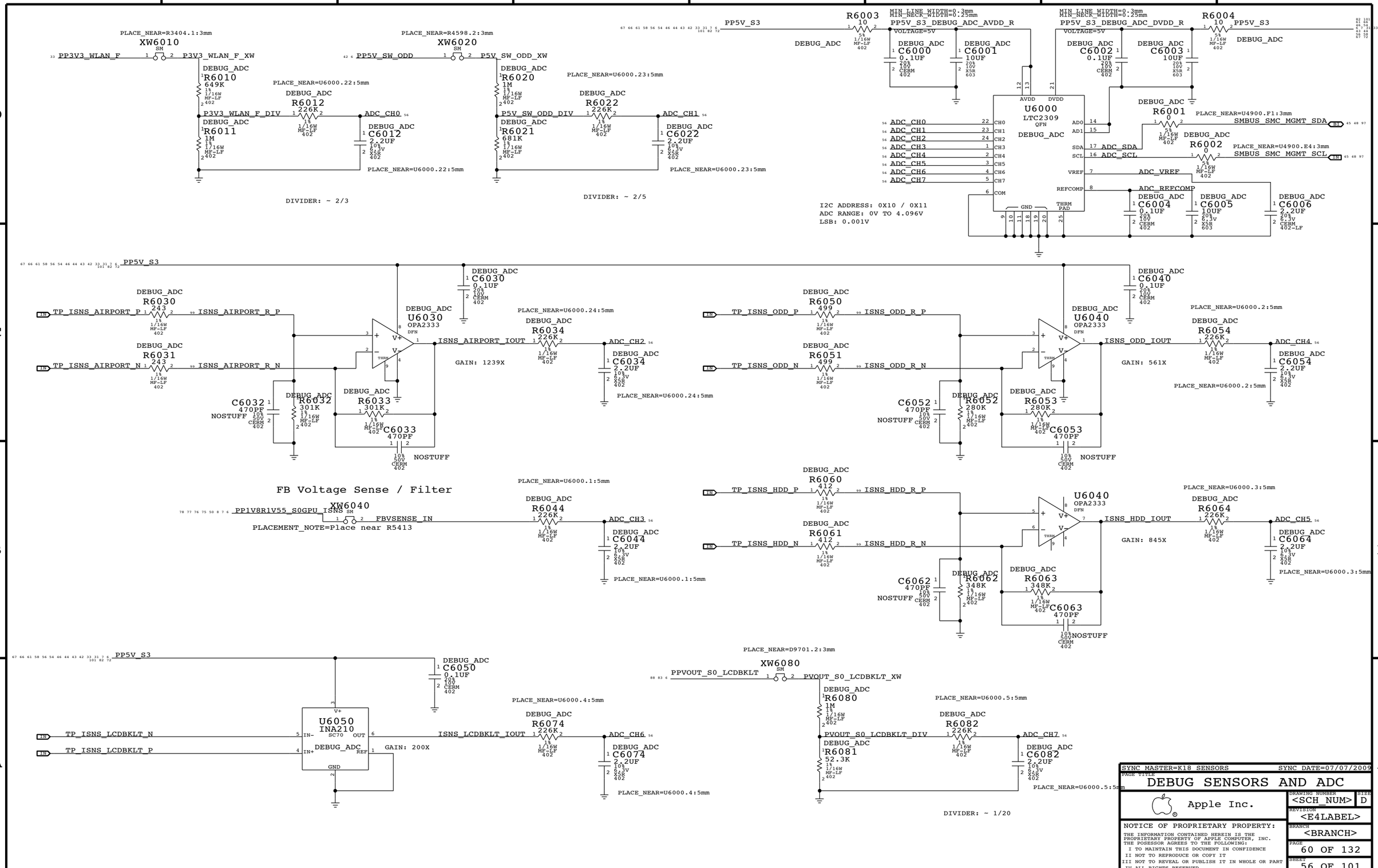

SYNC MASTER=K18 SENSORS SYNC DATE=07/07/2009

PAGE TITLE

DEBUG SENSORS AND ADC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 60 OF 132

SHEET 56 OF 101

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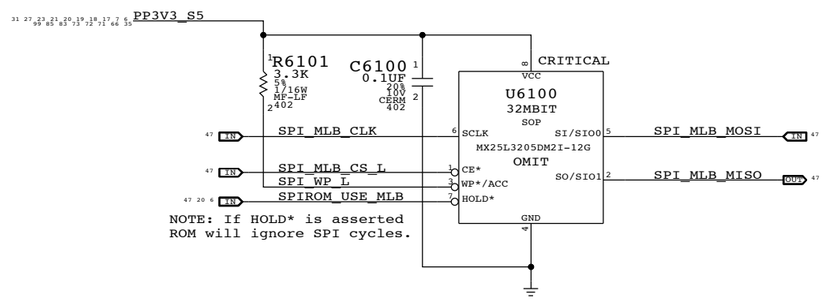

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

SPI ROM

Apple Inc.

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PAGE 61 OF 132

SHEET 57 OF 101

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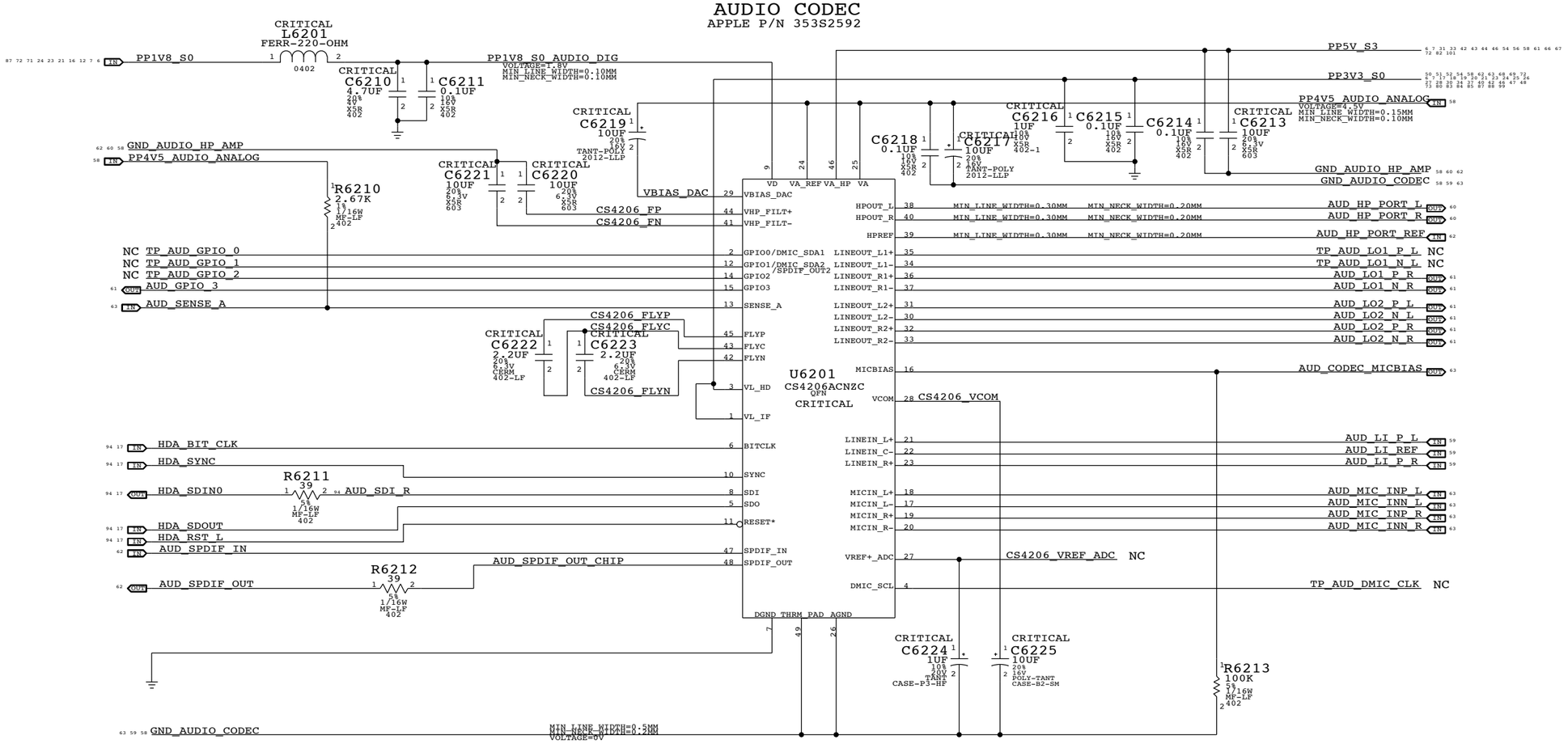
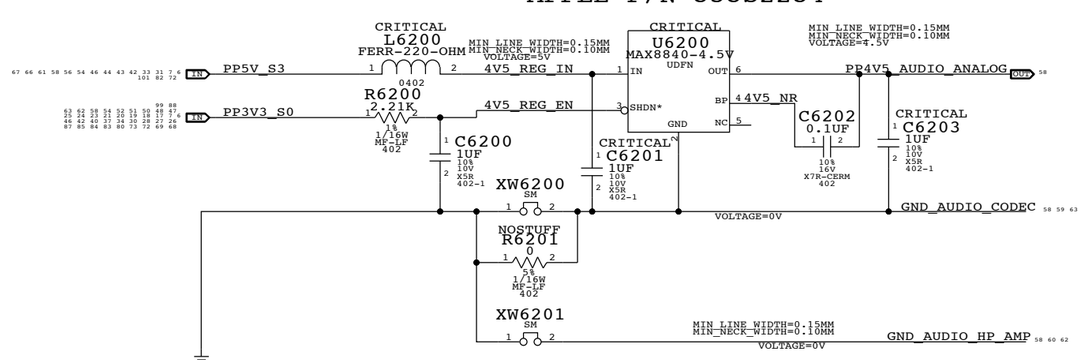
AUDIO CODEC
APPLE P/N 353S2592



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=K18 AUDIO SYNC DATE=09/21/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 62 OF 132
SHEET 58 OF 101

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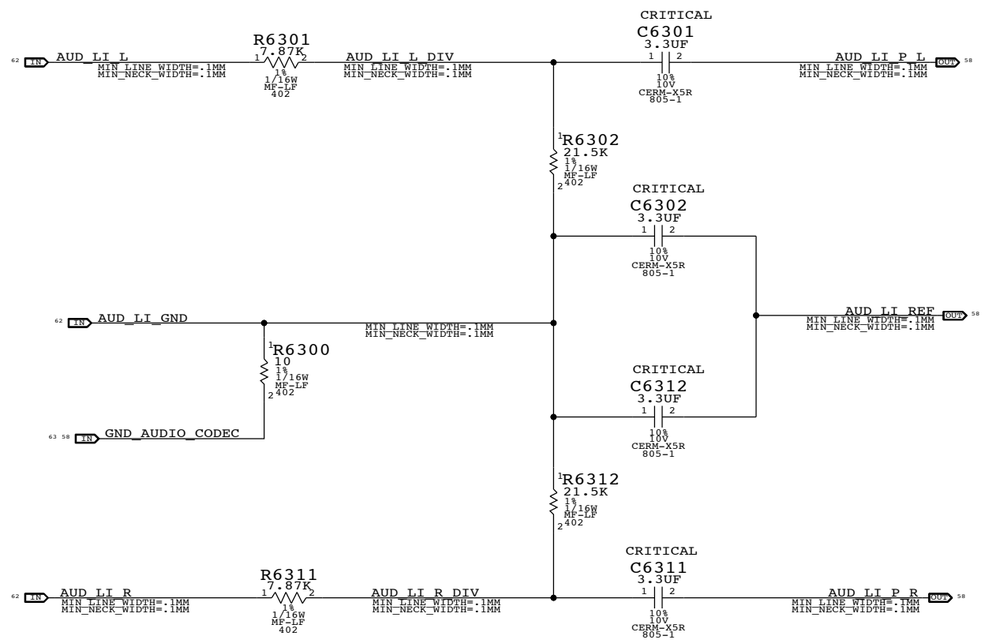
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC MASTER=K18 AUDIO SYNC DATE=07/29/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 63 OF 132
SHEET 59 OF 101

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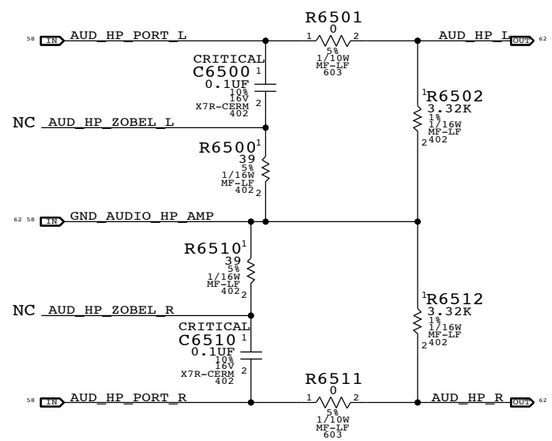
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER=K18 AUDIO SYNC DATE=07/29/2009

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 65 OF 132

SHEET 60 OF 101

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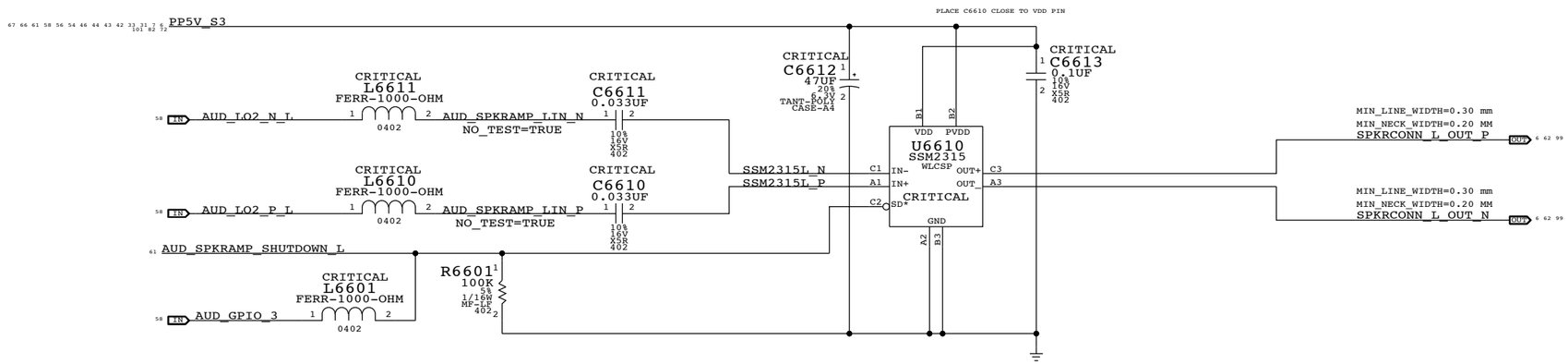
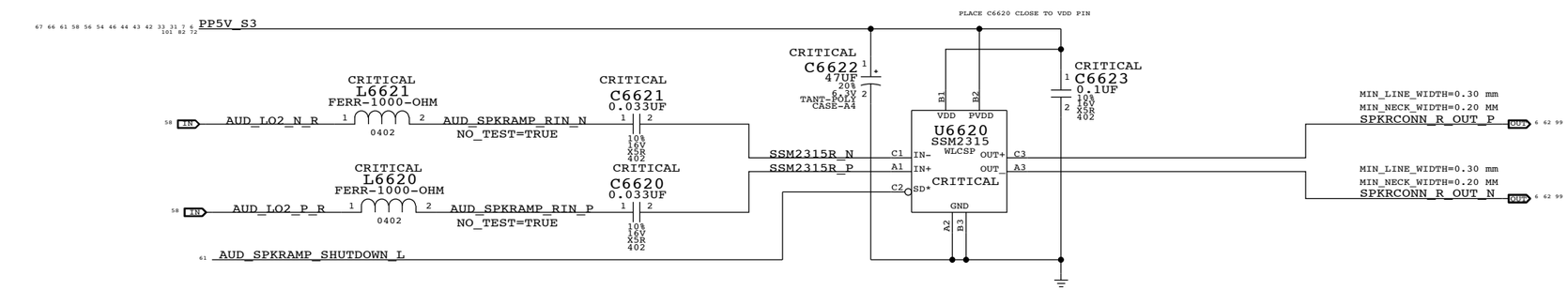
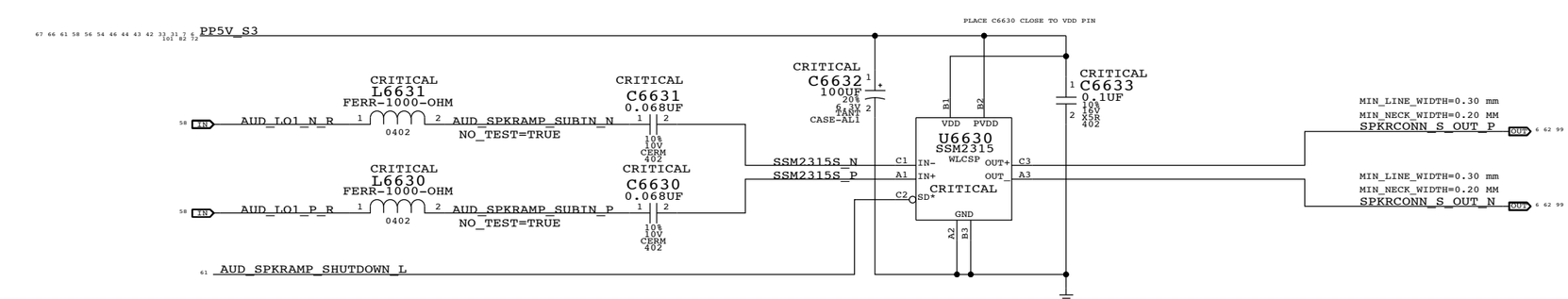
3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500

GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%







SYNC MASTER=K18 AUDIO SYNC DATE=07/29/2009

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 66 OF 132
SHEET 61 OF 101

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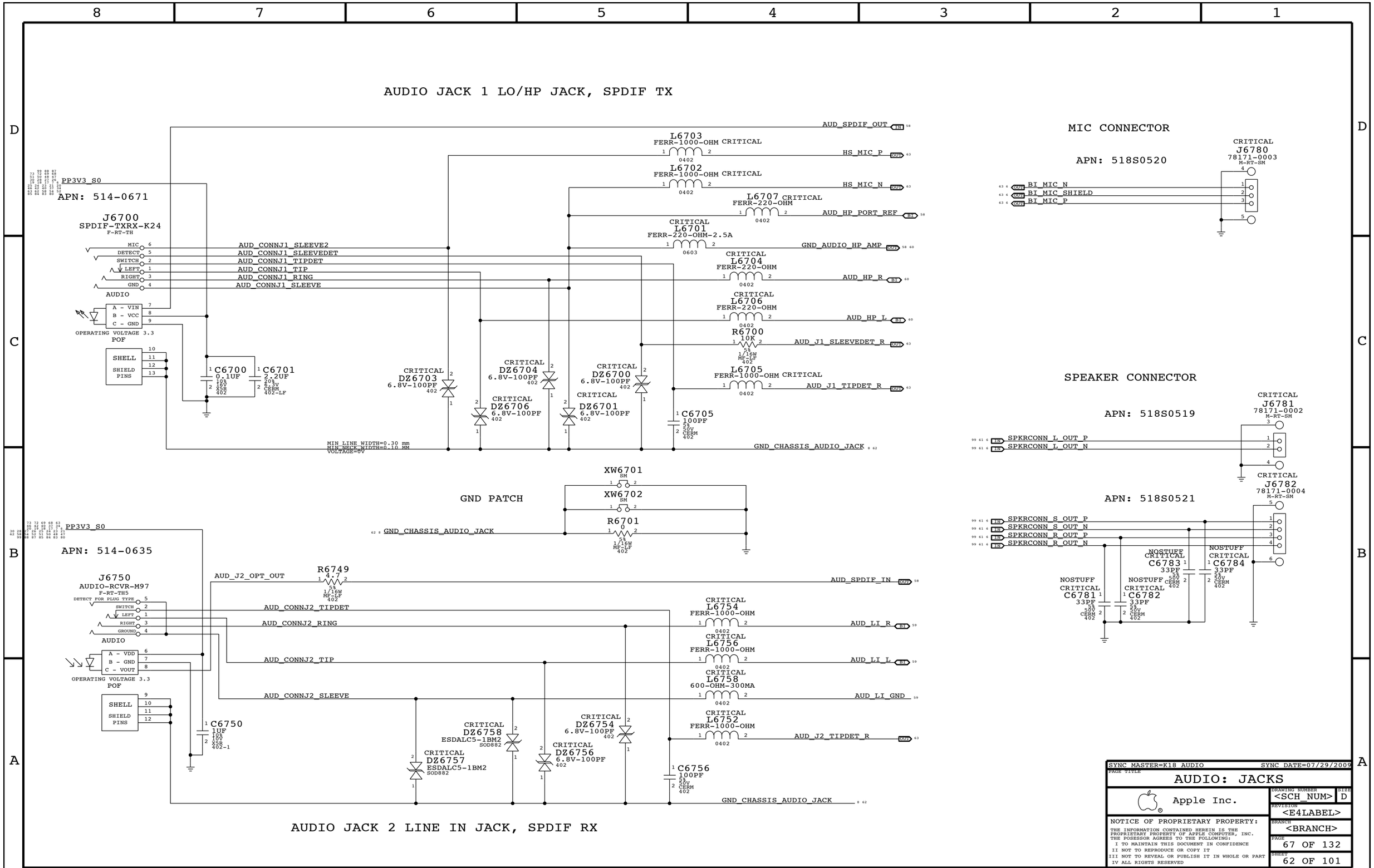
AUDIO JACK 1 LO/HP JACK, SPDIF TX
AUD_SPDIF_OUT
L6703 FERR-1000-OHM CRITICAL 0402
HS_MIC_P
L6702 FERR-1000-OHM CRITICAL 0402
HS_MIC_N
L6707 CRITICAL FERR-220-OHM 0402
AUD_HP_PORT_REF
CRITICAL L6701 FERR-220-OHM-2.5A 0603
GND_AUDIO_HP_AMP
CRITICAL L6704 FERR-220-OHM 0402
AUD_HP_R
CRITICAL L6706 FERR-220-OHM 0402
AUD_HP_L
R6700 10K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R
L6705 FERR-1000-OHM CRITICAL 0402
AUD_J1_TIPDET_R
PP3V3_S0
APN: 514-0671
J6700 SPDIF-TXRX-K24 F-RT-TH
MIC
DETECT
SWITCH
LEFT
RIGHT
GND
AUDIO
AUD_CONNJ1_SLEEVE2
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_CONNJ1_SLEEVE
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
C6700 0.1UF 10% 16V X5R 402
C6701 2.2UF 20% 6.3V CERM 402-LF
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6706 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402
C6705 100PF 5% 50V CERM 402
MIN LINE WIDTH=0.30 mm
MIN NECK WIDTH=0.10 MM
VOLTAGE=0V
GND_CHASSIS_AUDIO_JACK
GND PATCH
XW6701 SM
XW6702 SM
R6701 0 5% 1/16W MF-LF 402
GND_CHASSIS_AUDIO_JACK
PP3V3_S0
APN: 514-0635
J6750 AUDIO-RCVR-M97 F-RT-TH5
DETECT FOR PLUG TYPE
SWITCH
LEFT
RIGHT
GROUND
AUDIO
A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
C6750 1UF 10% 10V X5R 402-1
AUD_J2_OPT_OUT
R6749 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_IN
AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_TIP
AUD_CONNJ2_SLEEVE
CRITICAL L6754 FERR-1000-OHM 0402
AUD_LI_R
CRITICAL L6756 FERR-1000-OHM 0402
AUD_LI_L
CRITICAL L6758 600-OHM-300MA 0402
AUD_LI_GND
CRITICAL L6752 FERR-1000-OHM 0402
AUD_J2_TIPDET_R
CRITICAL DZ6758 ESDALC5-1BM2 SOD882
CRITICAL DZ6757 ESDALC5-1BM2 SOD882
CRITICAL DZ6754 6.8V-100PF 402
CRITICAL DZ6756 6.8V-100PF 402
C6756 100PF 5% 50V CERM 402
GND_CHASSIS_AUDIO_JACK
AUDIO JACK 2 LINE IN JACK, SPDIF RX
MIC CONNECTOR
APN: 518S0520
CRITICAL J6780 78171-0003 M-RT-SM
BI_MIC_N
BI_MIC_SHIELD
BI_MIC_P
SPEAKER CONNECTOR
APN: 518S0519
CRITICAL J6781 78171-0002 M-RT-SM
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
APN: 518S0521
CRITICAL J6782 78171-0004 M-RT-SM
SPKRCONN_S_OUT_P
SPKRCONN_S_OUT_N
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
NOSTUFF CRITICAL C6781 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6782 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6783 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6784 33PF 5% 50V CERM 402
SYNC MASTER=K18 AUDIO
SYNC DATE=07/29/2009
PAGE TITLE
AUDIO: JACKS
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
67 OF 132
SHEET
62 OF 101
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CODEC OUTPUT SIGNAL PATHS

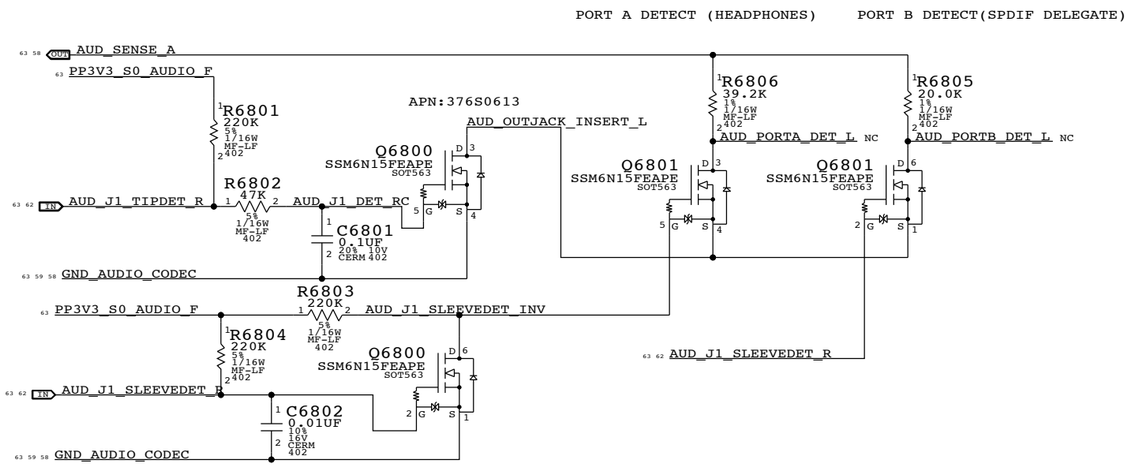
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

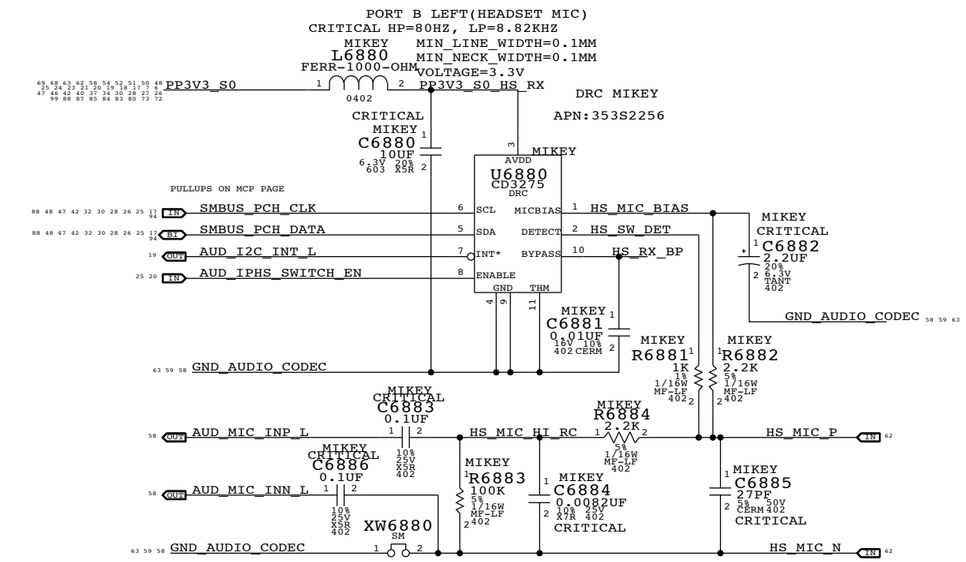
CODEC INPUT SIGNAL PATHS

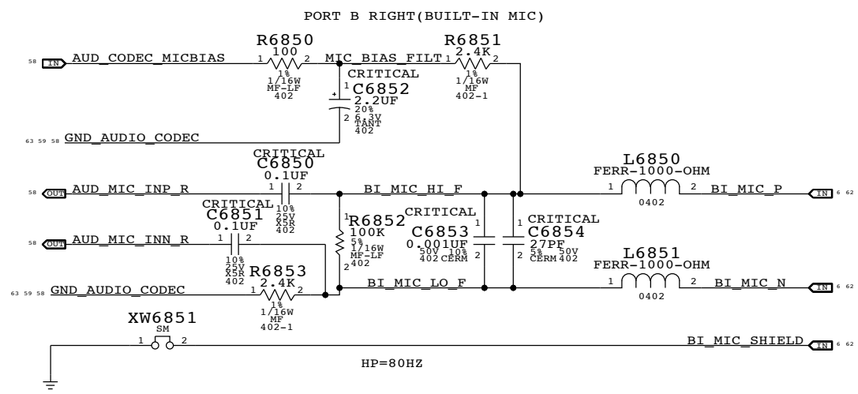
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

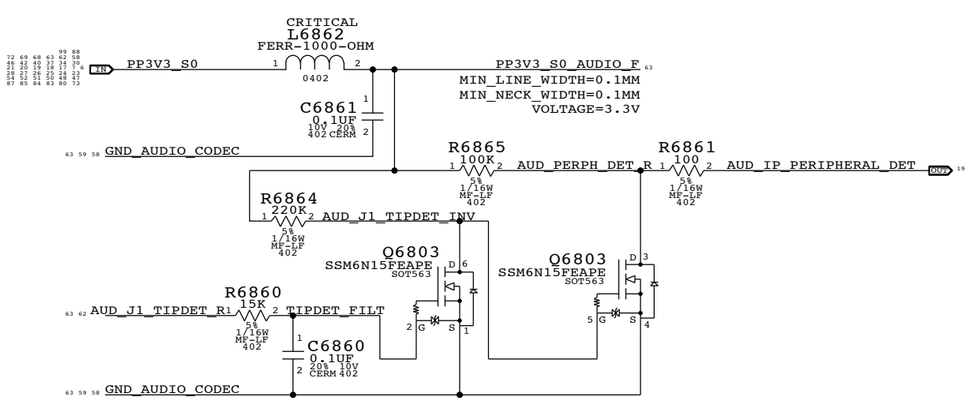
SYSTEM INT AND GPIO LINES

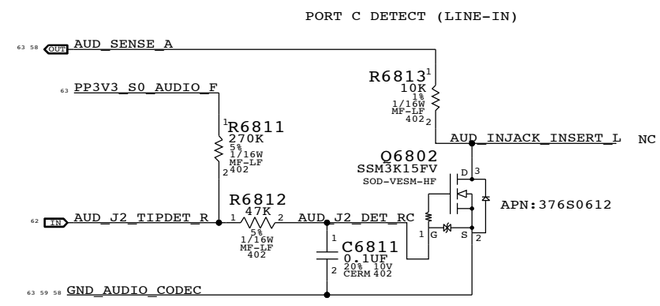
FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3











SYNC MASTER=K18 AUDIO SYNC DATE=07/29/2009

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 68 OF 132

SHEET 63 OF 101

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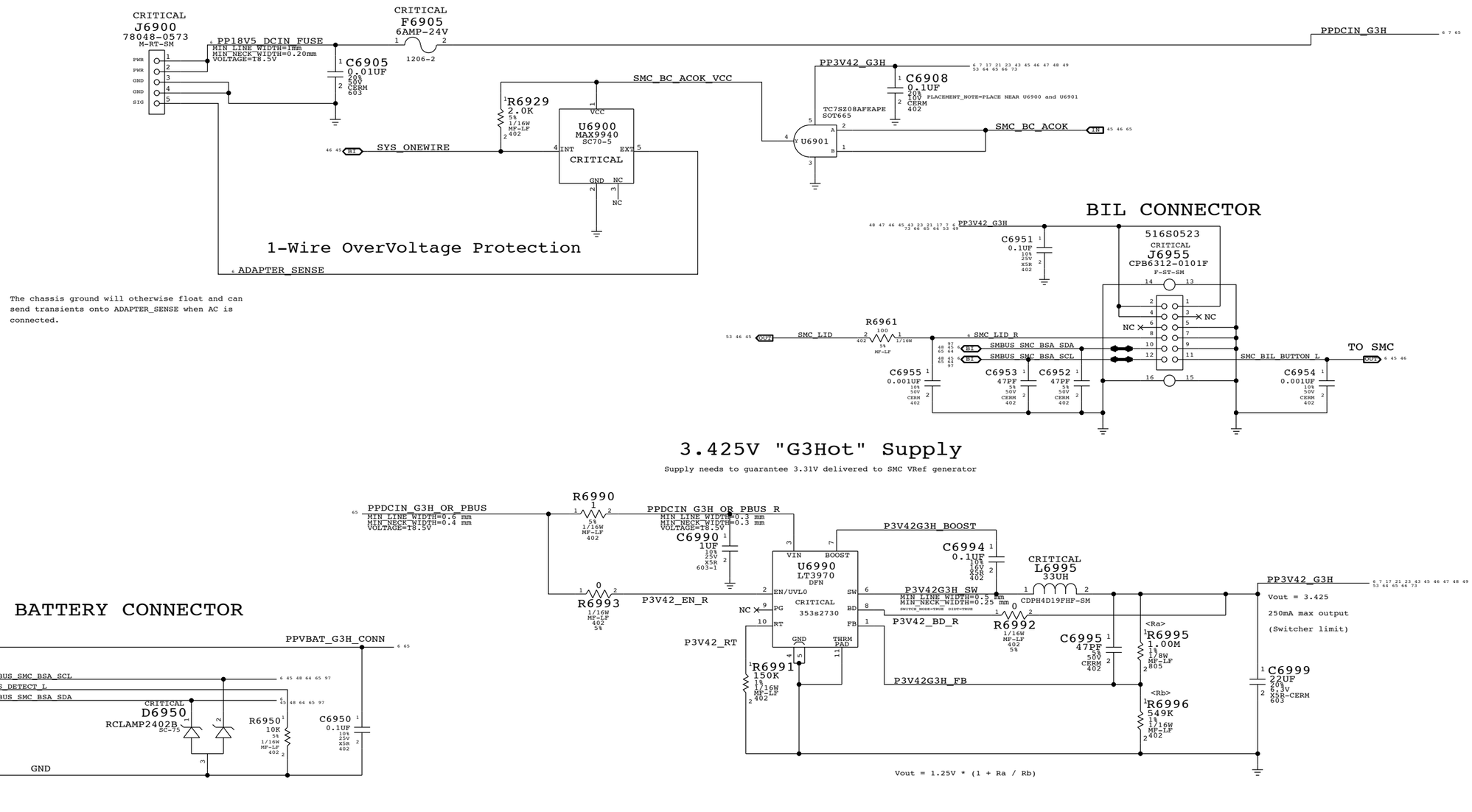
MagSafe DC Power Jack



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SYNC MASTER=K18 POWER SYNC DATE=06/30/2009

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

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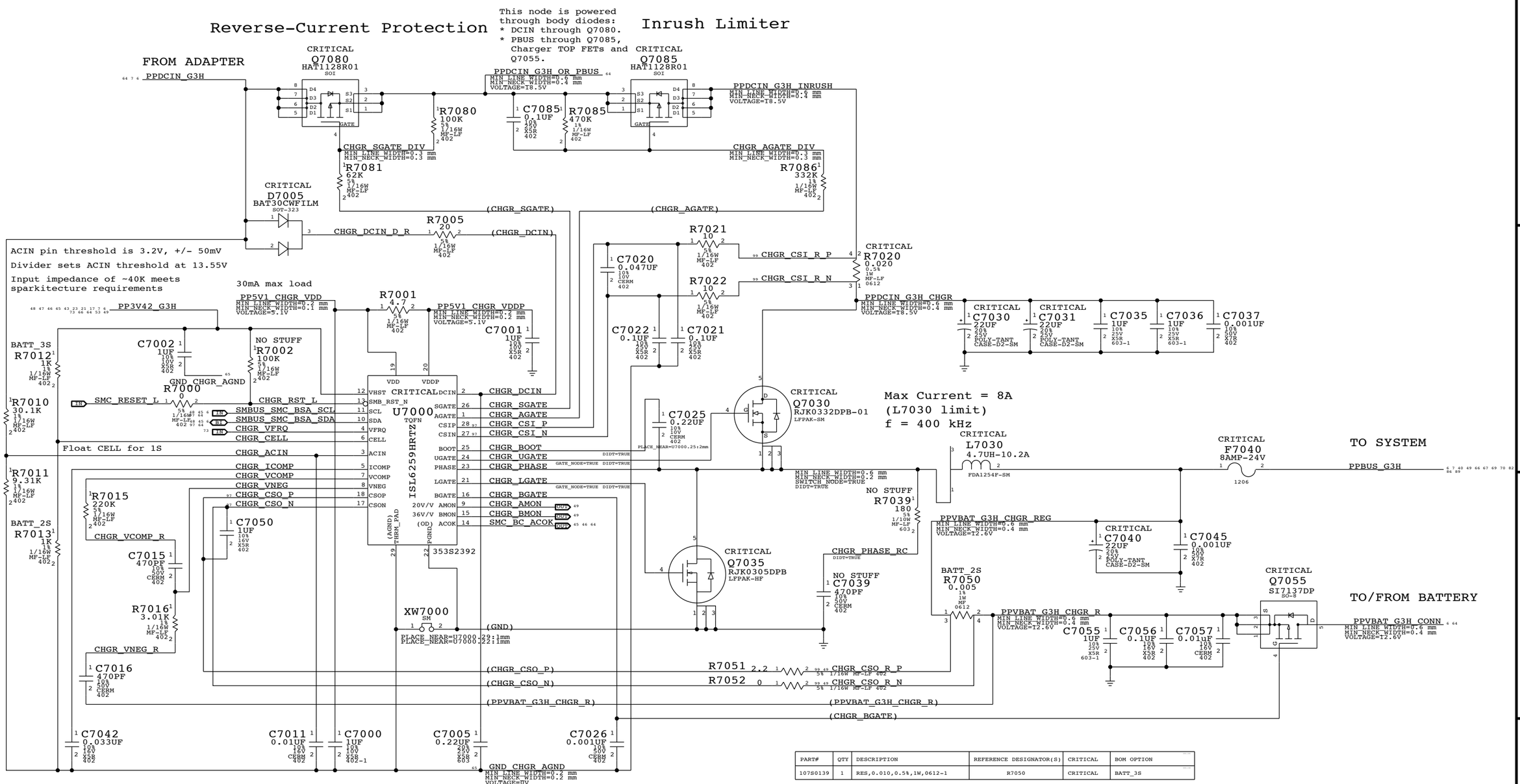
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 69 OF 132

SHEET 64 OF 101



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0139	1	RES,0.010,0.5%,1W,0612-1	R7050	CRITICAL	BATT_3S

SYNC MASTER=K18 POWER SYNC DATE=06/30/2009

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 70 OF 132
SHEET 65 OF 101

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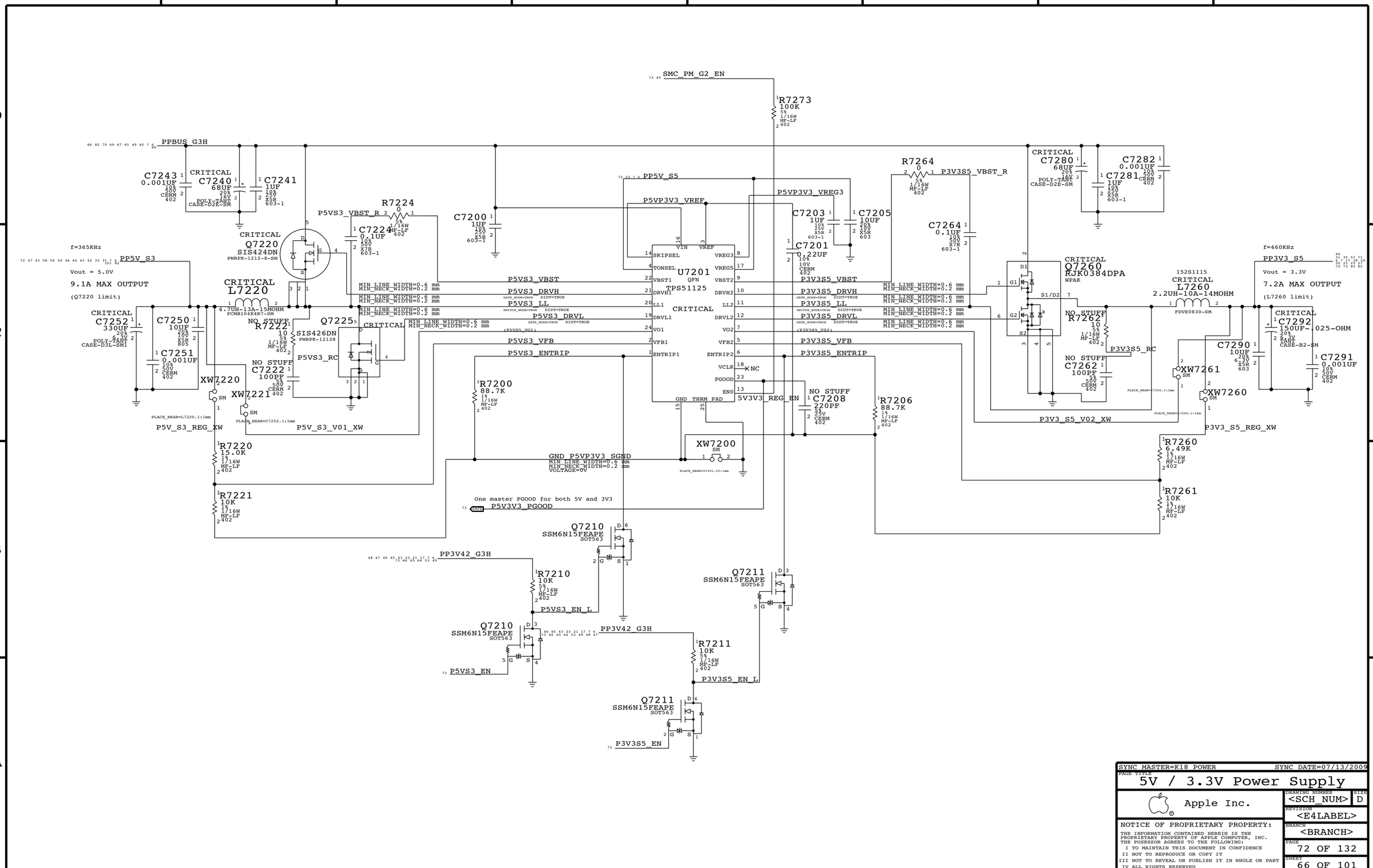

SYNC MASTER=K18 POWER SYNC DATE=07/13/2009

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 72 OF 132

SHEET 66 OF 101

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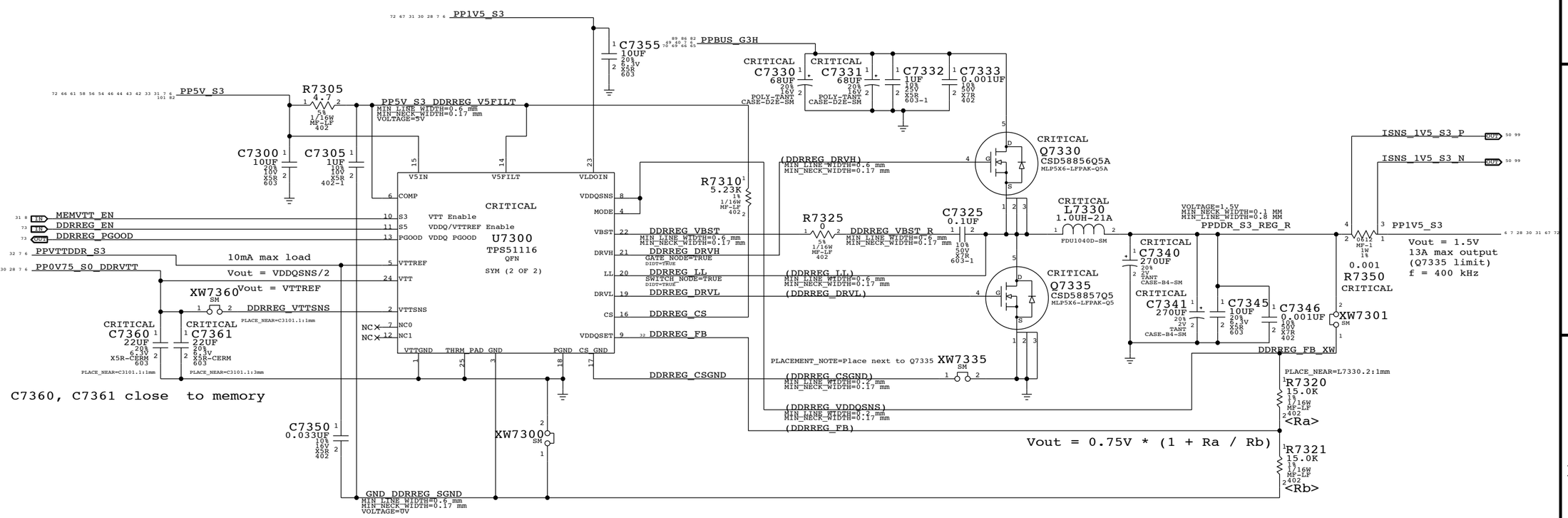

SYNC MASTER=K18 POWER SYNC DATE=07/14/2009

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 73 OF 132

SHEET 67 OF 101

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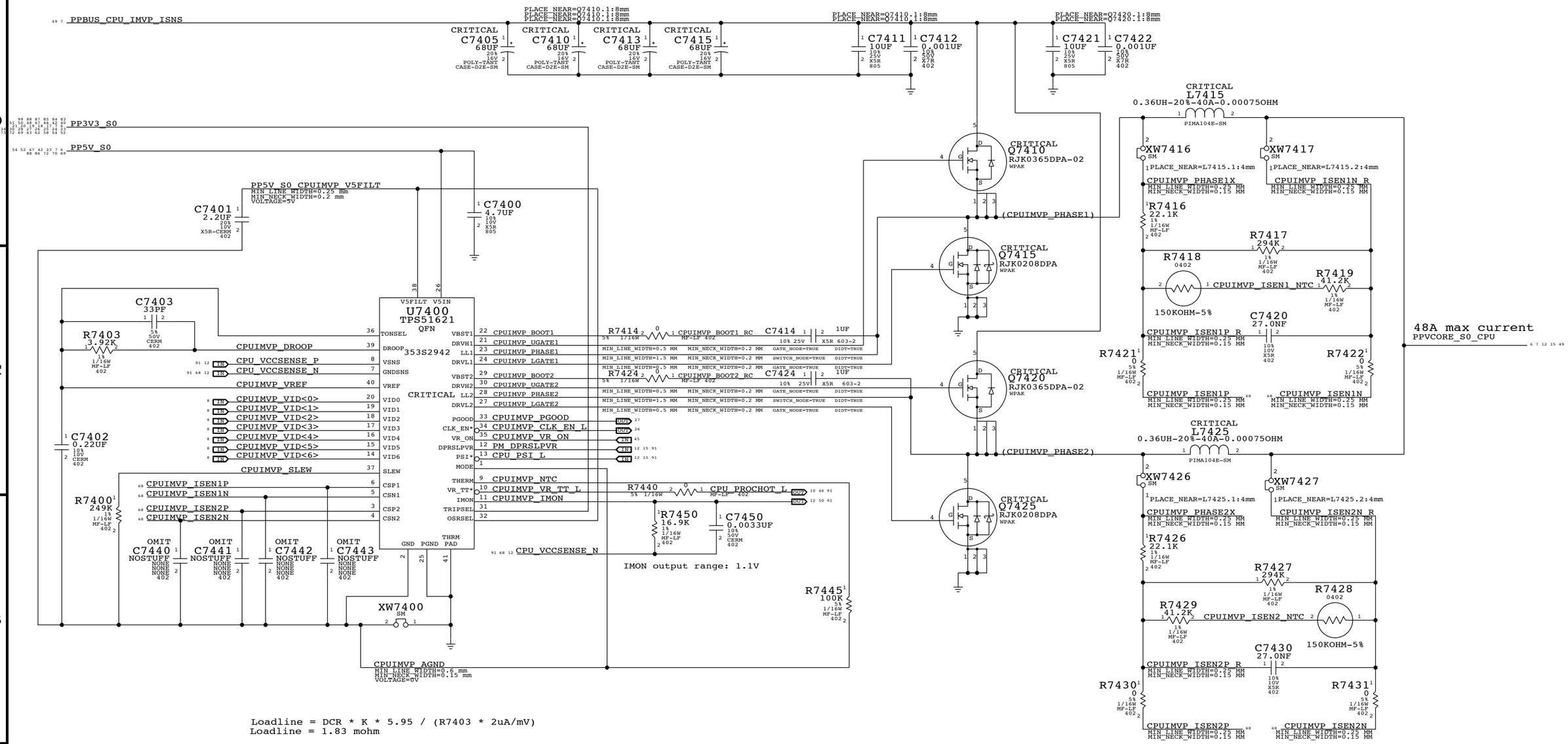

Loadline = DCR * K * 5.95 / (R7403 * 2uA/mV)
Loadline = 1.83 mohm

VIMON = Io * DCR * 2uA/mV * R7450
50 A = 1.00 V

K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.66

SYNC MASTER=K18 POWER SYNC DATE=06/29/2009

PAGE TITLE
CPU IMVP VCore Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 74 OF 132
SHEET 68 OF 101

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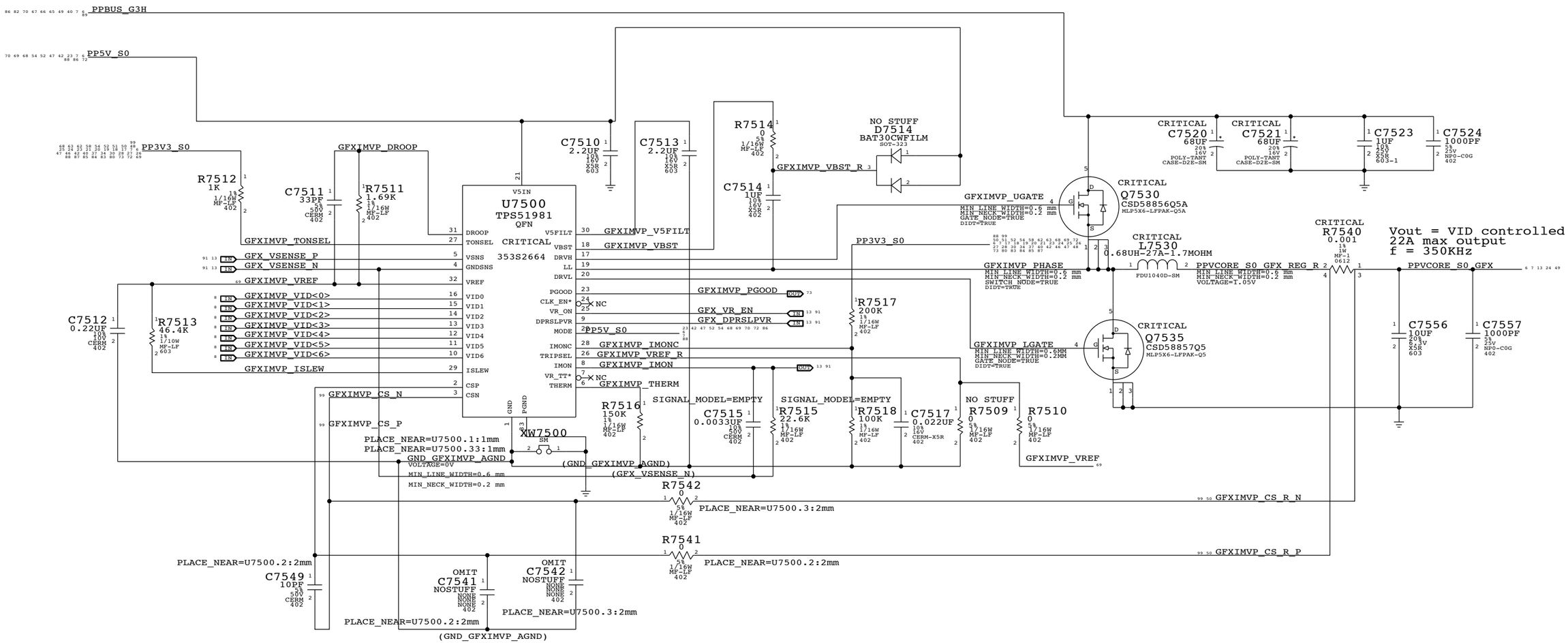
GFX IMVP VCORE



Imon= Io xR7540 x2uA/mV x R7515

Imon= Io x45.2mV/A

22A => 1V

SYNC MASTER=K18 POWER SYNC DATE=07/08/2009

PAGE TITLE
GFX IMVP VCore Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 75 OF 132

SHEET 69 OF 101

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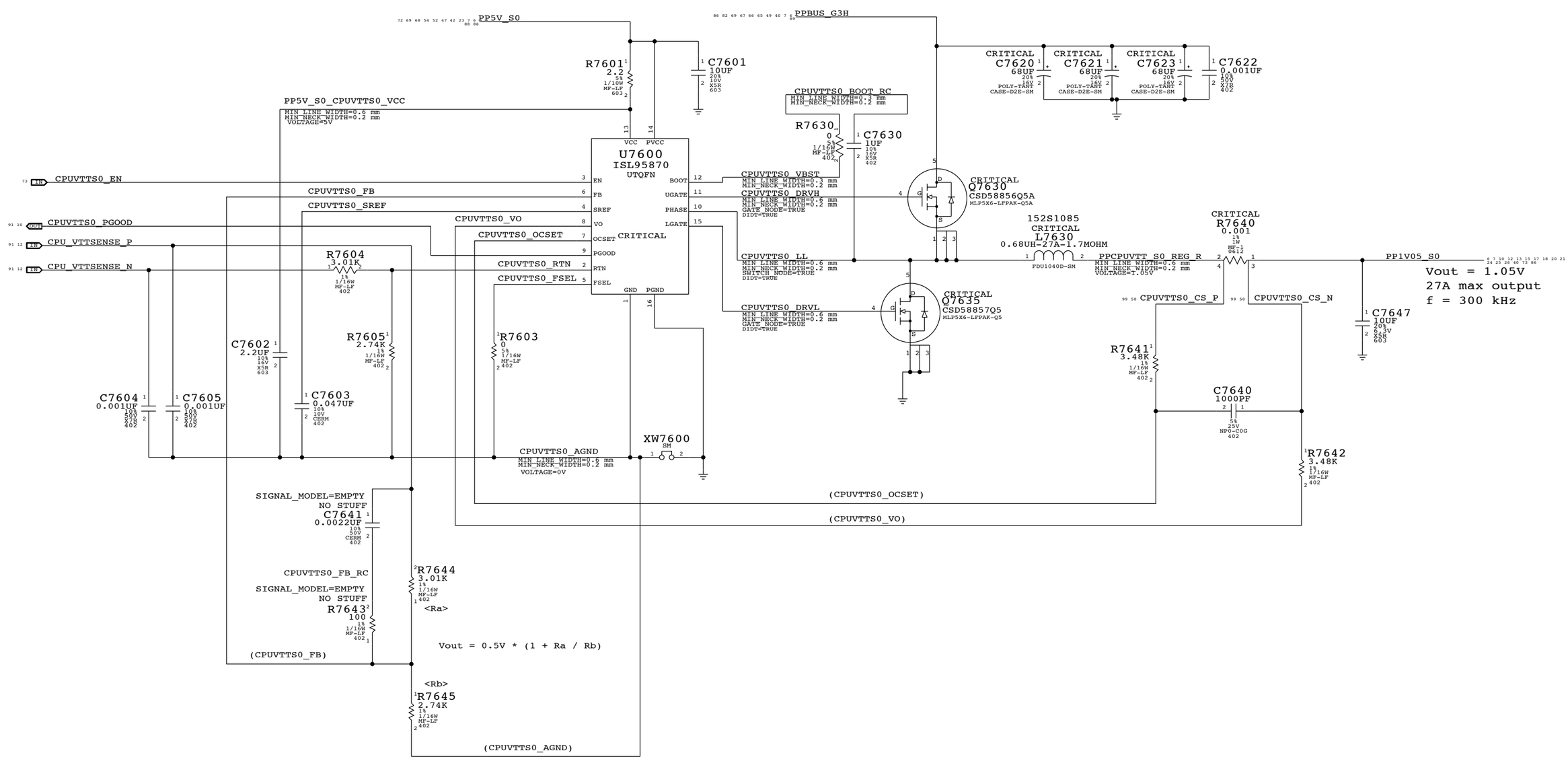
CPU VTT (1.05V S0) Regulator



SYNC MASTER=K18 POWER SYNC DATE=07/14/2009

PAGE TITLE
CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 76 OF 132

SHEET 70 OF 101

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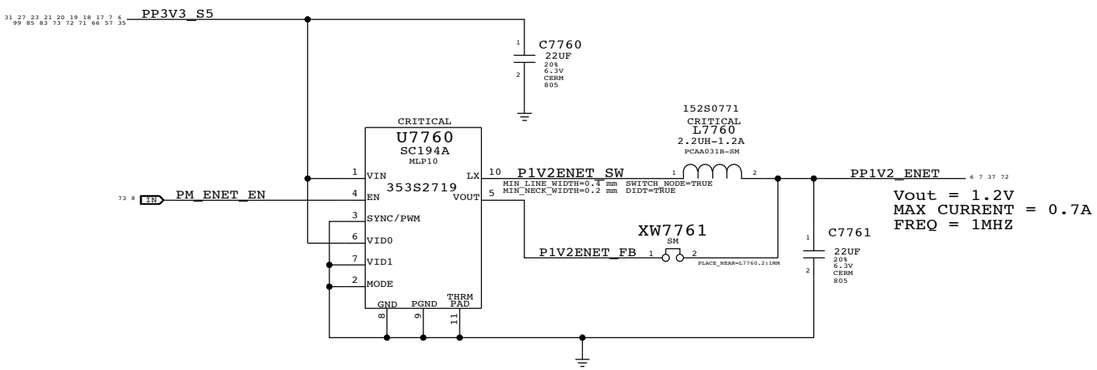
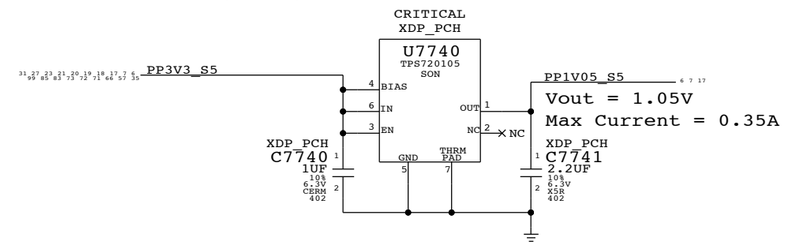
1.2V S3 Regulator

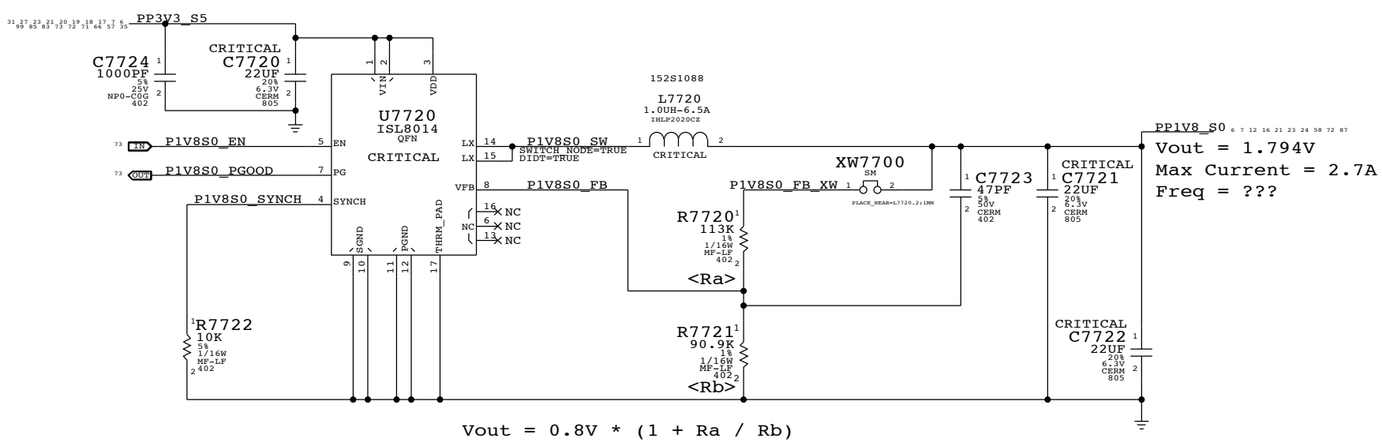


1.05V S5 LDO

Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.8V S0 Regulator



Vout = 0.8V * (1 + Ra / Rb)

SYNC MASTER=K18 POWER SYNC DATE=06/29/2009

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE 77 OF 132

SHEET 71 OF 101

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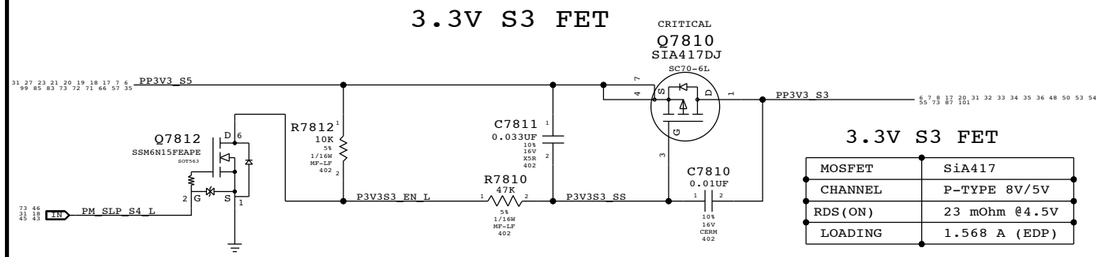
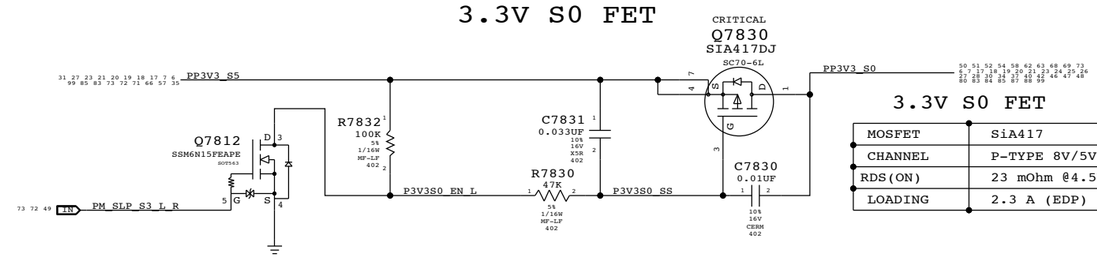
3.3V S3 FET



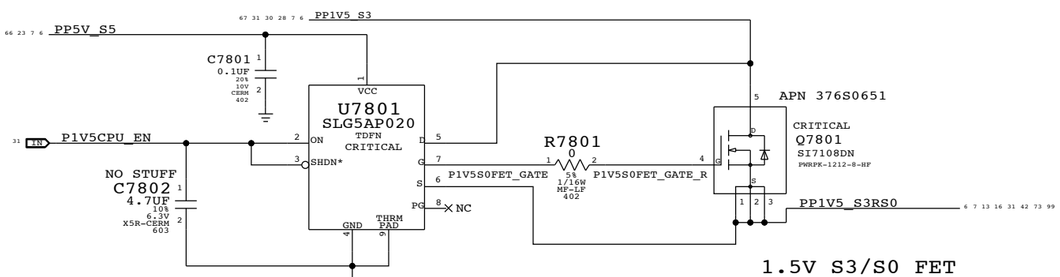
3.3V S3 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	1.568 A (EDP)

3.3V S0 FET



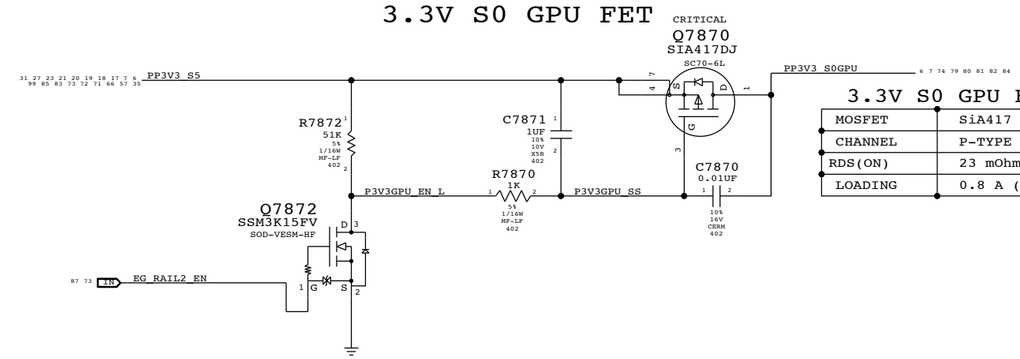
3.3V S0 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	2.3 A (EDP)

1.5V S3/S0 FET



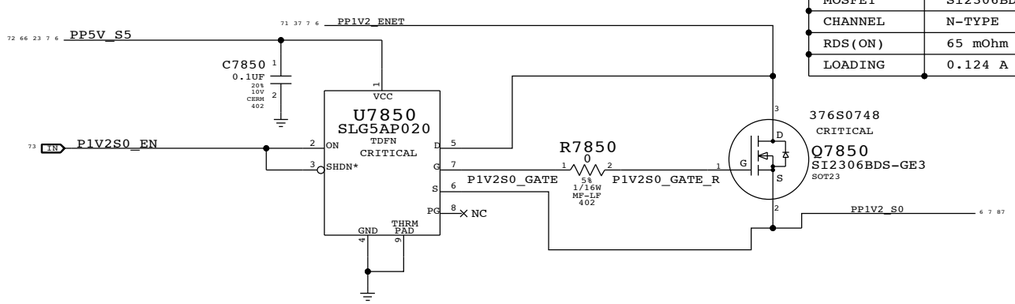
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	3.2 A (EDP)

3.3V S0 GPU FET



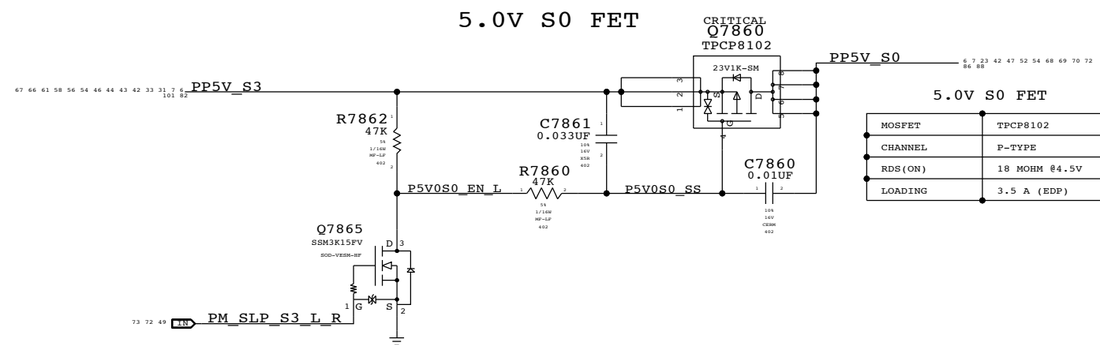
3.3V S0 GPU FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	0.8 A (EDP)

1.2V S0 FET



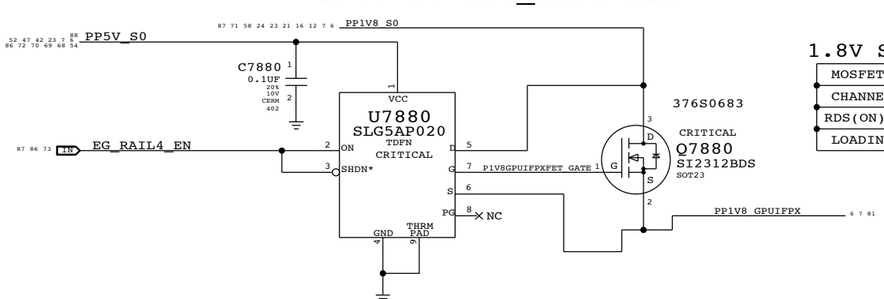
1.2V S0 FET	
MOSFET	SI2306BDS-GE3
CHANNEL	N-TYPE
RDS(ON)	65 mOhm @4.5V
LOADING	0.124 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	3.5 A (EDP)

1.8V S0 GPU_IFPX FET



1.8V S0 GPU_IFPX FET	
MOSFET	SI2312BDS
CHANNEL	N-TYPE
RDS(ON)	31 mOhm @4.5V
LOADING	0.3 A (EDP)

SYNC MASTER=K18 POWER SYNC DATE=06/10/2009

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 78 OF 132

SHEET 72 OF 101

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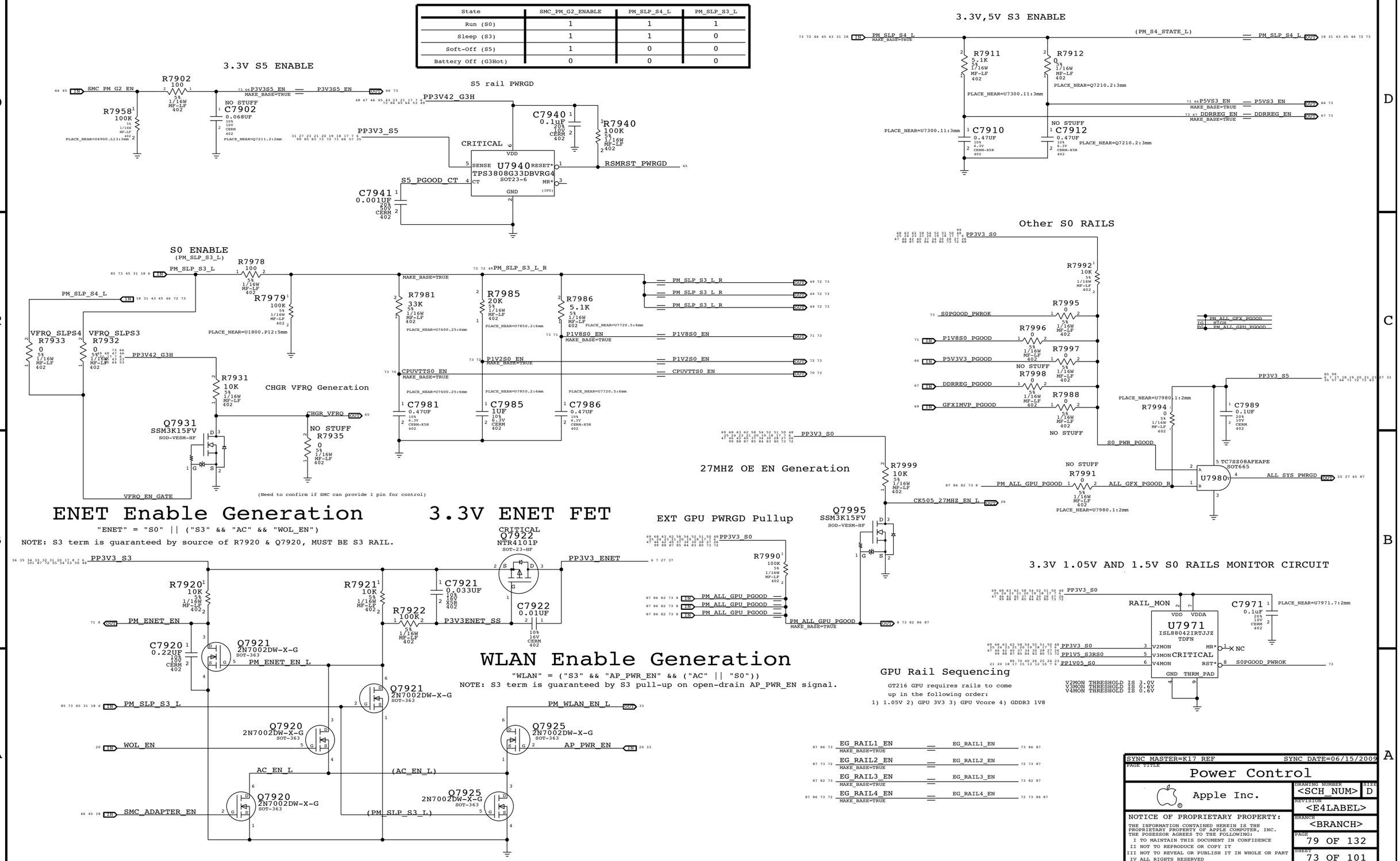
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

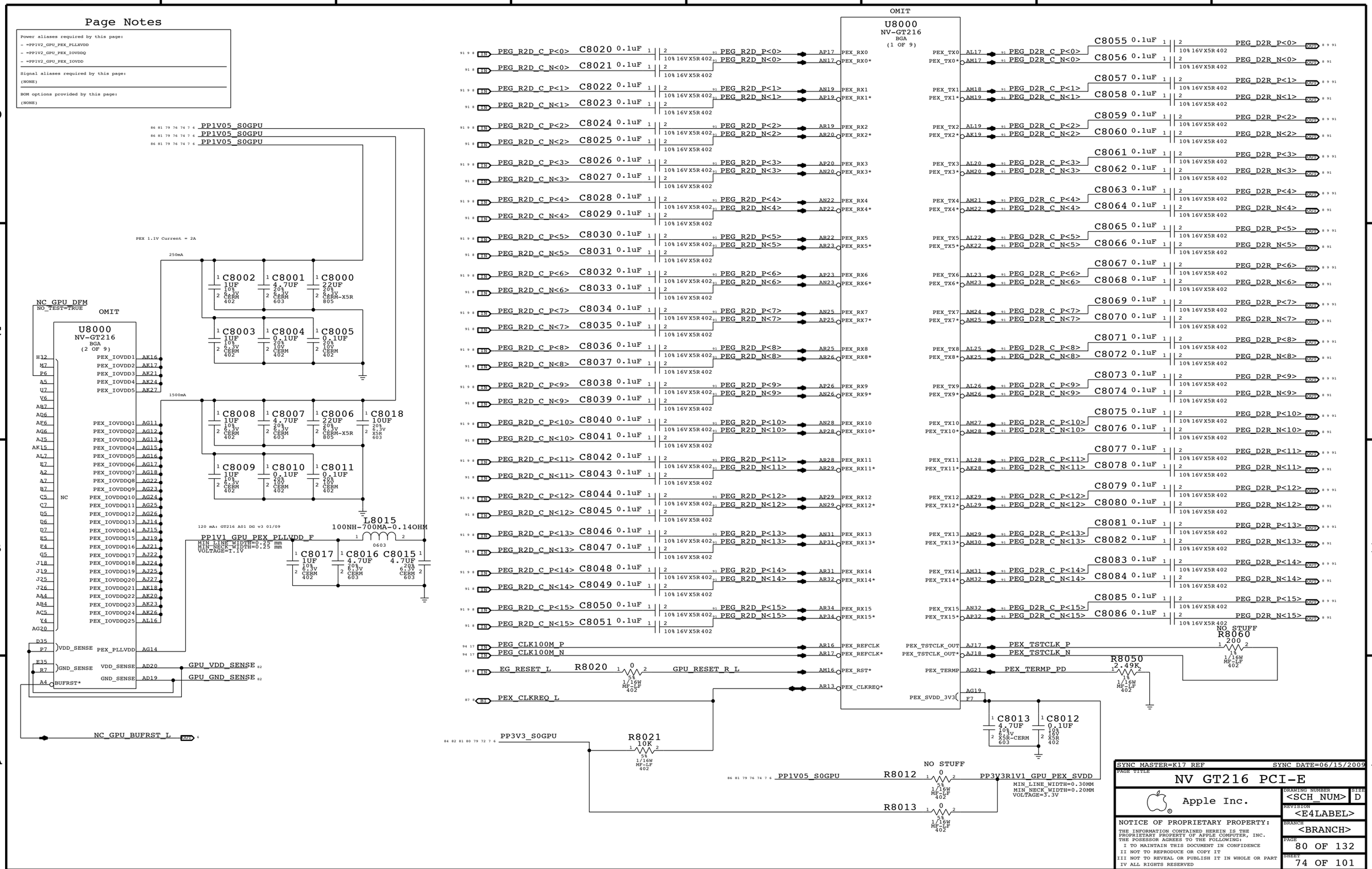


Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
NV GT216 PCI-E

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 80 OF 132
SHEET 74 OF 101

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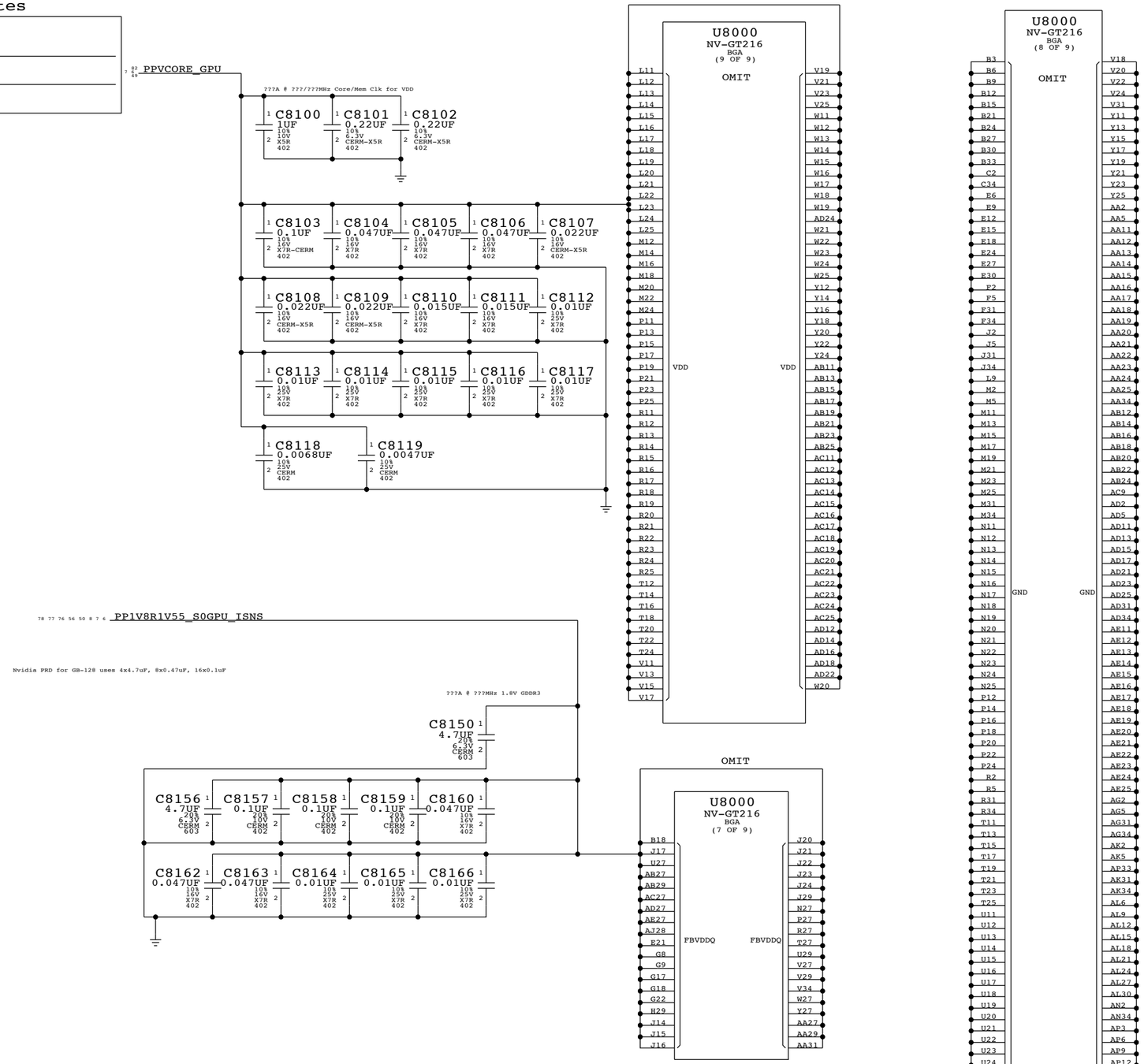
Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
NV GT216 CORE/FB POWER

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PAGE 81 OF 132

SHEET 75 OF 101

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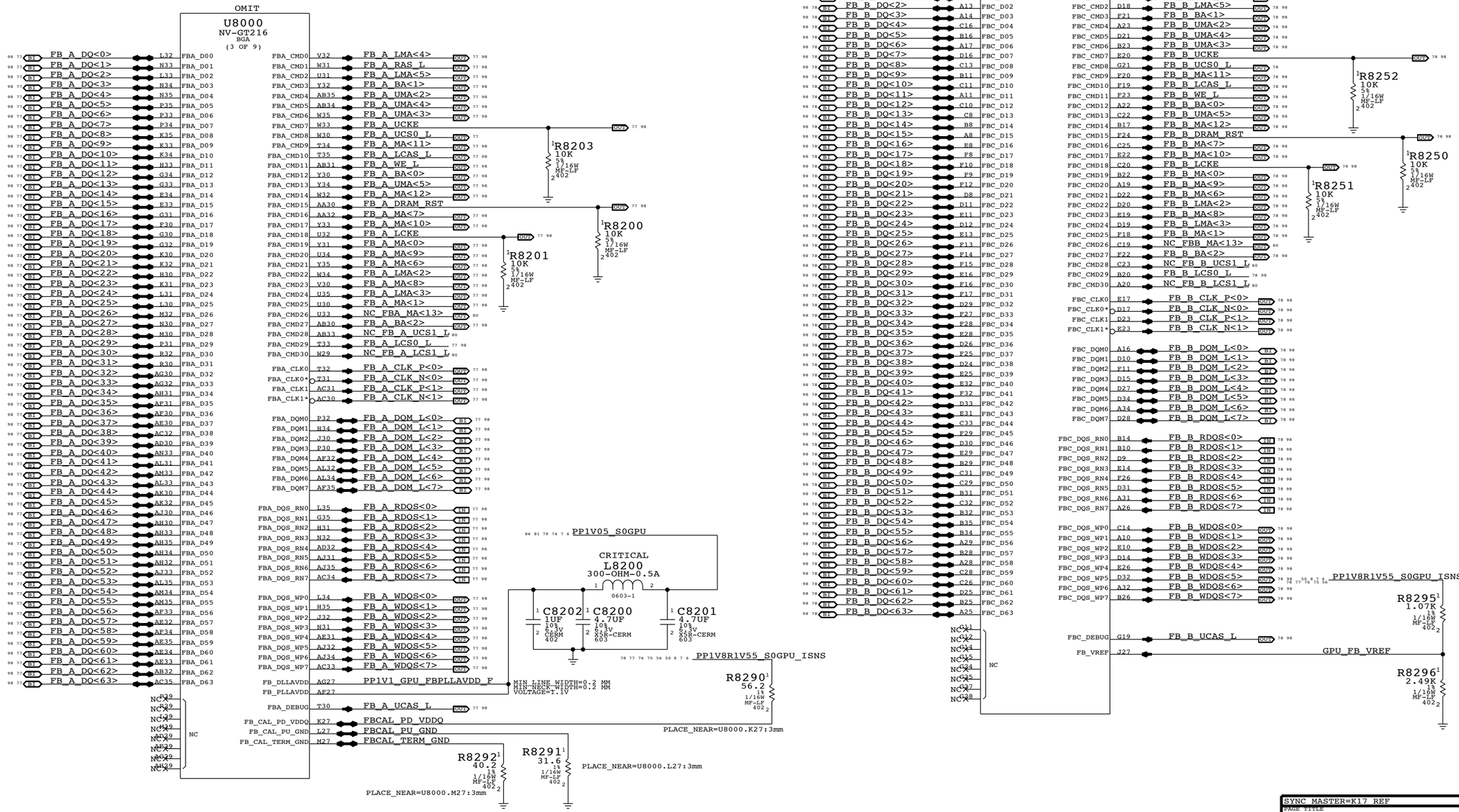
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
NV GT216 FRAME BUFFER I/F

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PAGE 82 OF 132

SHEET 76 OF 101

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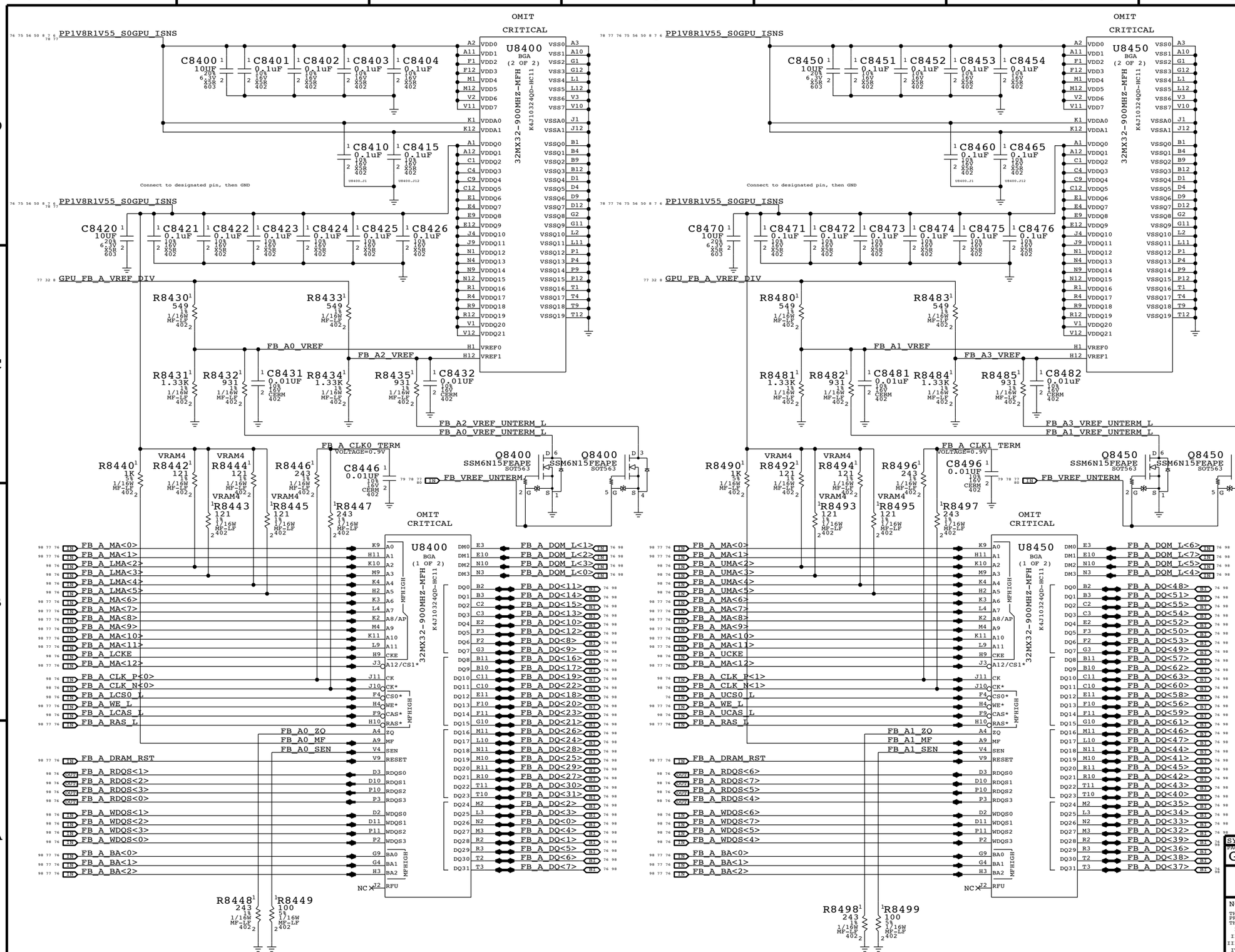

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
GDDR3 Frame Buffer A (Top)

Apple Inc.

DRAWING NUMBER	SIZE
<SCH_NUM>	D
REVISION <E4LABEL>	
BRANCH <BRANCH>	
PAGE 84 OF 132	
SHEET 77 OF 101	

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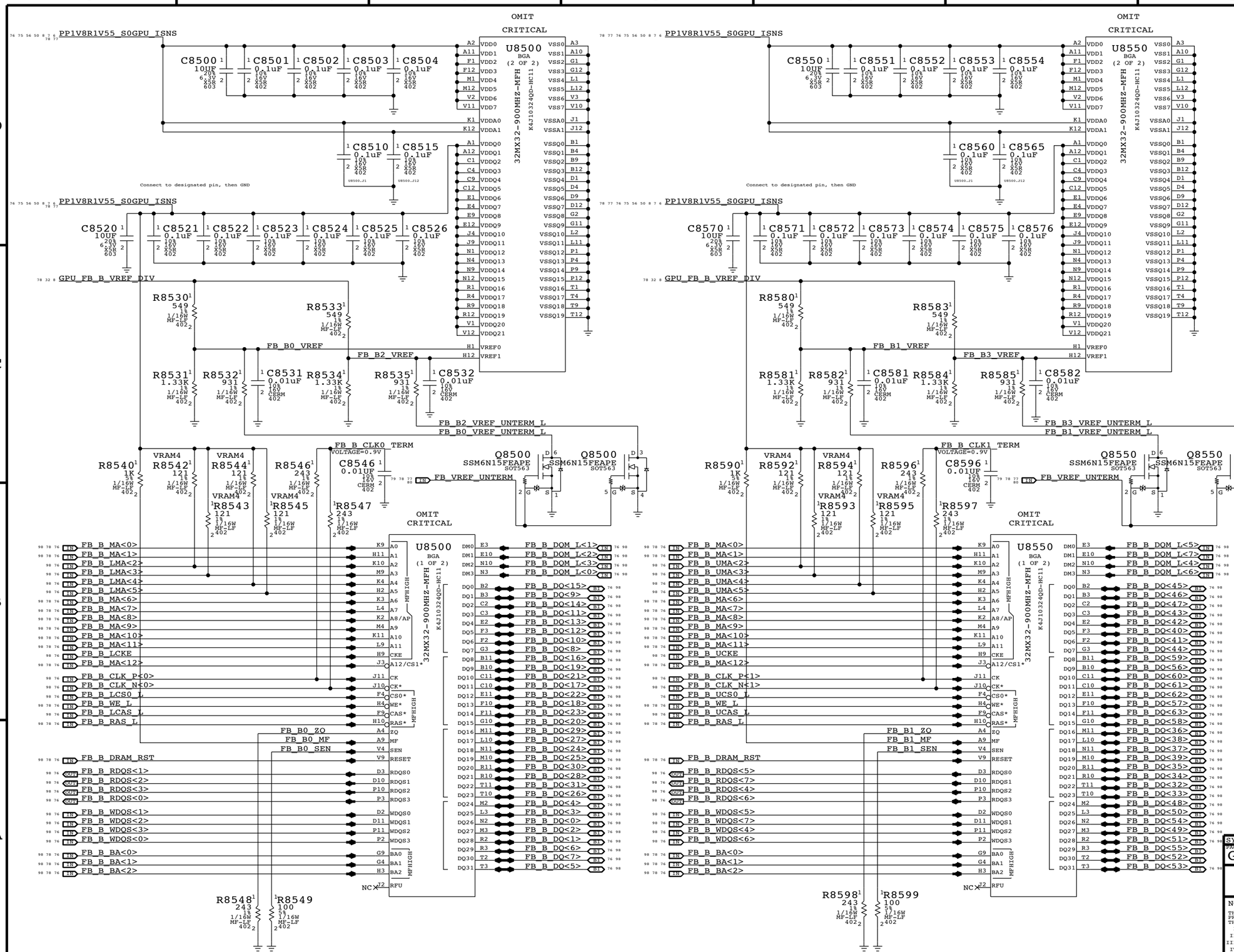

Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

GDDR3 Frame Buffer B (Top)

Apple Inc.

DRAWING NUMBER	SIZE
<SCH_NUM>	D
REVISION <E4LABEL>	
BRANCH <BRANCH>	
PAGE 85 OF 132	
SHEET 78 OF 101	

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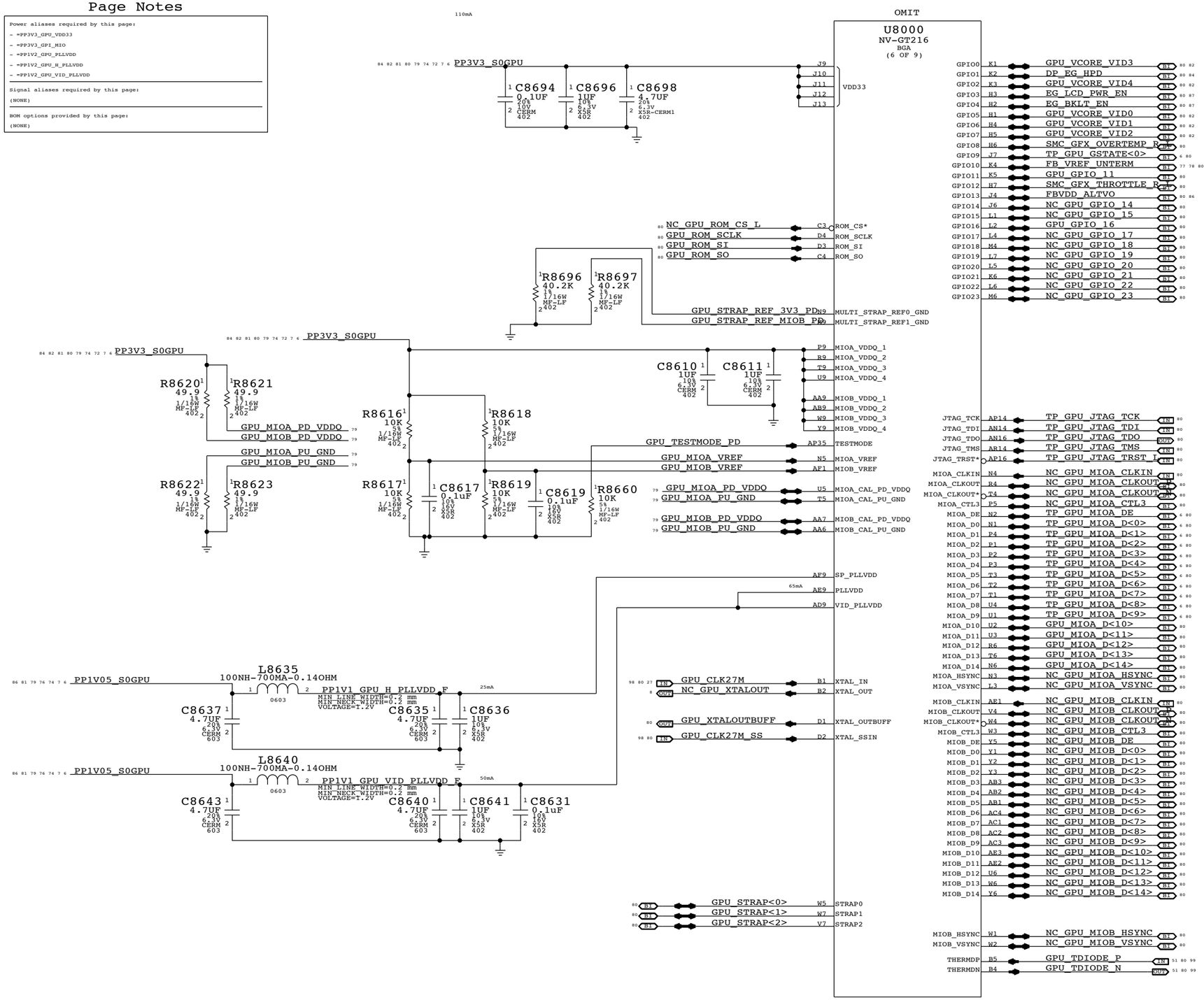
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
NV GT216 GPIO/MIO/MISC

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 86 OF 132
SHEET 79 OF 101

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GPIOs

Signal	Native Func	Signal
GPU_VCORE_VID3	GP	GPU_VCORE_VID3
DP_EG_HPD	HPDC	DP_EG_HPD
GPU_VCORE_VID4	LCD0_BL_PWM	GPU_VCORE_VID4
EG_LCD_PWR_EN	LCD0_VDD	EG_LCD_PWR_EN
EG_BKLT_EN	LCD0_BL_EN	EG_BKLT_EN
GPU_VCORE_VID0	VID0	GPU_VCORE_VID0
GPU_VCORE_VID1	VID1	GPU_VCORE_VID1
GPU_VCORE_VID2	VID2/MEM_VID	GPU_VCORE_VID2
SMC_GFX_OVERTEMP_R_L	SHDTEMP	SMC_GFX_OVERTEMP_R_L
TP_GPU_GSTATE<0>	FAN_PWM	TP_GPU_GSTATE<0>
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM
GPU_GPIO_11	SLI_SYNC	TP_GPU_GSTATE<1>
SMC_GFX_THROTTLE_R_L	PC_BRT	SMC_GFX_THROTTLE_R_L
FBVDD_ALTVO	PWR_CTL0	FBVDD_ALTVO
NC_GPU_GPIO_14	PWR_CTL1	NC_GPU_GPIO_14

GPIOs

Signal	Native Func	Signal
NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23

Renamed signals

Signal	Signal
GPU_CLK27M	GPU_CLK27M
GPU_CLK27M_SS	GPU_CLK27M_SS
GPU_TDIODE_P	GPU_TDIODE_P
GPU_TDIODE_N	GPU_TDIODE_N
LVDS_EG_DDC_CLK	LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA	LVDS_EG_DDC_DATA
DP_EG_DDC_CLK	DP_EG_DDC_CLK
DP_EG_DDC_DATA	DP_EG_DDC_DATA

Unused signals

Signal	Signal
TP_GPU_JTAG_TCK	TP_GPU_JTAG_TCK
TP_GPU_JTAG_TDI	TP_GPU_JTAG_TDI
TP_GPU_JTAG_TDO	TP_GPU_JTAG_TDO
TP_GPU_JTAG_TMS	TP_GPU_JTAG_TMS
TP_GPU_JTAG_TRST_L	TP_GPU_JTAG_TRST_L
NC_FBA_MA<13>	NC_FBA_MA<13>
NC_FBB_MA<13>	NC_FBB_MA<13>

Unused I2C Buses

Signal	Signal
NC_GPU_I2CC_SCL	NC_GPU_I2CC_SCL
NC_GPU_I2CC_SDA	NC_GPU_I2CC_SDA
NC_GPU_I2CH_SCL	NC_GPU_I2CH_SCL
NC_GPU_I2CH_SDA	NC_GPU_I2CH_SDA

I2CS ties into SMBus connection page

(I2CS requires pullups even if not used)

Signal	Signal
NC_FB_B_UCS1_L	NC_FB_B_UCS1_L
NC_FB_B_LCS1_L	NC_FB_B_LCS1_L
NC_GPU_ROM_CS_L	NC_GPU_ROM_CS_L
NC_FB_A_UCS1_L	NC_FB_A_UCS1_L
NC_FB_A_LCS1_L	NC_FB_A_LCS1_L
NC_LVDS_EG_B_CLK_P	NC_LVDS_EG_B_CLK_P
NC_LVDS_EG_B_CLK_N	NC_LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3>	NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>	NC_LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3>	NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>	NC_LVDS_EG_B_DATA_N<3>

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

Signal	Signal
NC_GPU_MIOA_CLKOUT_P	NC_GPU_MIOA_CLKOUT_P
NC_GPU_MIOA_CLKOUT_N	NC_GPU_MIOA_CLKOUT_N
NC_GPU_MIOA_CTL3	NC_GPU_MIOA_CTL3
TP_GPU_MIOA_DE	TP_GPU_MIOA_DE
TP_GPU_MIOA_D<9..0>	GPU_MIOA_D<9..0>
NC_GPU_MIOA_CLKIN	NC_GPU_MIOA_CLKIN
NC_GPU_MIOA_D<14..10>	GPU_MIOA_D<14..10>
NC_GPU_MIOA_HSYNC	NC_GPU_MIOA_HSYNC
NC_GPU_MIOA_VSYNC	NC_GPU_MIOA_VSYNC
NC_GPU_MIOB_CLKIN	NC_GPU_MIOB_CLKIN
NC_GPU_MIOB_CLKOUT_P	NC_GPU_MIOB_CLKOUT_P
NC_GPU_MIOB_CLKOUT_N	NC_GPU_MIOB_CLKOUT_N
NC_GPU_MIOB_CTL3	NC_GPU_MIOB_CTL3
NC_GPU_MIOB_DE	NC_GPU_MIOB_DE
NC_GPU_MIOB_D<14..0>	GPU_MIOB_D<14..0>
NC_GPU_MIOB_VSYNC	NC_GPU_MIOB_VSYNC
NC_GPU_MIOB_HSYNC	NC_GPU_MIOB_HSYNC

Unused Clocks

GPU_CLK27M_SS

GPU_XTALOUTBUFF

R8780[1] 10K 5% 1/16W MF-LF 402 — GPU_SS_INT — R8781[1] 10K 5% 1/16W MF-LF 402

Config Straps

PP3V3_S0GPU

	OMIT	NO STUFF	NO STUFF
	R8707[1] 2.0K 5% 1/16W MF-LF 402	R8709[1] 4.99K 1% 1/16W MF-LF 402	R8711[1] 15.0K 1% 1/16W MF-LF 402
	GPU_ROM_SI (OUT)		
	GPU_ROM_SO (IN)		
	GPU_ROM_SCLK (IN)		
	OMIT		
	R8708[1] 45.3K 1% 1/16W MF-LF 402	R8710[1] 10K 1% 1/16W MF-LF 402	R8712[1] 15.0K 1% 1/16W MF-LF 402

PP3V3_S0GPU

R8701[1] 45.3K 1% 1/16W MF-LF 402	R8703[1] 34.8K 1% 1/16W MF-LF 402	R8705[1] 10K 1% 1/16W MF-LF 402
GPU_STRAP<0> (B1)		
GPU_STRAP<1> (B1)		
GPU_STRAP<2> (B1)		
NO STUFF	NO STUFF	NO STUFF
R8702[1] 2.0K 5% 1/16W MF-LF 402	R8704[1] 10K 1% 1/16W MF-LF 402	R8706[1] 24.9K 1% 1/16W MF-LF 402

Physical

Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0]	PU/PD	Rval
0 0000	PD	5k
1 0001	PD	10k
2 0010	PD	15k (HYN 256)
3 0011	PD	20k (SAM 256)
4 0100	PD	25k (SAM 512)
5 0101	PD	30k
6 0110	PD	35k (HYN 512)
7 0111	PD	45k

Strap S1/S2 Bit[3:0]	PU/PD	Rval
8 1000	PU	5k
9 1001	PU	10k
A 1010	PU	15k
B 1011	PU	20k
C 1100	PU	25k
D 1101	PU	30k
E 1110	PU	35k
F 1111	PU	45k

PCI_DEVID[4:0]=0x14

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0353	1	RES,MTL FILM,1/16W,24.9K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX

PP3V3_S0

PP3V3_S0GPU

R8750[1] 2.2K 5% 1/16W MF-LF 402	R8751[1] 2.2K 5% 1/16W MF-LF 402	R8752[1] 4.7K 5% 1/16W MF-LF 402	R8753[1] 4.7K 5% 1/16W MF-LF 402
DP_EG_DDC_CLK (IN)			
DP_EG_DDC_DATA (BI)			
DP_IG_DDC_CLK (IN)			
DP_IG_DDC_DATA (BI)			

PP3V3_S0GPU

R8796[1] 2.2K 5% 1/16W MF-LF 402	R8797[1] 2.2K 5% 1/16W MF-LF 402	
SMC_GFX_OVERTEMP_R_L	R8798 0 NO STUFF 5% 1/16W MF-LF 402	SMC_GFX_OVERTEMP_L (OUT)
SMC_GFX_THROTTLE_R_L	R8799 0 5% 1/16W MF-LF 402	SMC_GFX_THROTTLE_L (OUT)
		EG_LCD_PWR_EN (OUT)
		EG_BKLT_EN (OUT)
		FBVDD_ALTVO (OUT)
		FB_VREF_UNTERM (OUT)
R8792[1] 10K 5% 1/16W MF-LF 402	R8793[1] 10K 5% 1/16W MF-LF 402	R8794[1] 10K 5% 1/16W MF-LF 402	NO STUFF R8795[1] 10K 5% 1/16W MF-LF 402

PP3V3_S0GPU

DP_CA_DET_EG_FET — R8742[1] 100K 1% 1/16W MF-LF 402 — DP_CA_DET_EG_FET

Q8742 SOD-VESM-HF SSM3K15FV

EG_DP_CA_DET — DP_CA_DET (IN)

R8743 0 5% 1/16W MF-LF 402 — DP_CA_DET_EG (IN)

DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

SYNC MASTER=K17 REF — SYNC DATE=06/15/2009

PAGE TITLE: GT216 GPIOS & STRAPS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 87 OF 132

SHEET: 80 OF 101

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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

72 7 6 PP1V8_GPUIFPX

CRITICAL
L8800
300-OHM-0.5A
0603-1

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402 (Place at AG9)
C8803 0.1UF 20% 10V CERM 402 (Place at AG10)

?mA peak per diff pair
?mA peak for all pairs

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

81 79 76 74 7 6 84 PP1V05_S0GPU

GPU_IFPEF_RSET 81
GPU_IFPC_RSET 81
GPU_IFPAB_RSET 81
GPU_IFPD_RSET 81

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402
R8858 1K 1% 1/16W MF-LF 402

L8805
180-OHM-1.5A
0603

80mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 1UF 10% 6.3V CERM 402

PP1V1_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

86 81 79 76 74 7 6 PP1V05_S0GPU

L8810
180-OHM-1.5A
0603

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402 (Place at AJ8)
C8813 0.1UF 20% 10V CERM 402 (Place at AK8)

?mA peak per diff pair
?mA peak for all pairs

PP1V1_GPU_IFPCD_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815
300-OHM-0.5A
0603-1

84 82 81 80 79 74 72 7 6 PP3V3_S0GPU

160mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 1UF 10% 6.3V CERM 402

PP3V3_GPU_IFPC_PLLVDD_F 81
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

PP1V8_GPU_IFPEF_PLLVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V
Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

U8000
NV-GT216
BGA
(5 OF 9)

Pin	Signal	Pin	Signal
AG9	IFPA_IOVDD	AM11	IFPA_TXC
AG10	IFPB_IOVDD	AM12	IFPA_TXC*
AJ8	IFPC_IOVDD	AN8	IFPA_TXD0
AK8	IFPD_IOVDD	AL8	IFPA_TXD0*
AE7	IFPE_IOVDD	AM10	IFPA_TXD1
AD7	IFPF_IOVDD	AN9	IFPA_TXD1*
AK9	IFPAB_PLLVDD	AK10	IFPA_TXD2
AJ11	IFPAB_RSET	AL10	IFPA_TXD2*
AJ9	IFPC_PLLVDD	AK11	IFPA_TXD3
AK7	IFPC_RSET	AL11	IFPA_TXD3*
AJ6	IFPEF_PLLVDD	AP13	IFPB_TXC
AL1	IFPEF_RSET	AN13	IFPB_TXC*
G1	I2CA_SCL	AN8	IFPB_TXD4
G4	I2CA_SDA	AP8	IFPB_TXD4*
E3	I2CC_SCL	AP10	IFPB_TXD5
E4	I2CC_SDA	AN10	IFPB_TXD5*
E2	I2CS_SCL	AR11	IFPB_TXD6
E1	I2CS_SDA	AR10	IFPB_TXD6*
F6	I2CH_SCL	AN11	IFPB_TXD7
G6	I2CH_SDA	AP11	IFPB_TXD7*
G3	I2CB_SCL	AP2	IFPC_AUX_I2CW_SCL
G2	I2CB_SDA	AN3	IFPC_AUX_I2CW_SDA*
		AM7	IFPC_L0
		AM6	IFPC_L0*
		AL5	IFPC_L1
		AM5	IFPC_L1*
		AM3	IFPC_L2
		AM4	IFPC_L2*
		AP1	IFPC_L3
		AR2	IFPC_L3*
		AR4	IFPD_AUX_I2CX_SCL
		AN4	IFPD_AUX_I2CX_SDA*
		AR8	IFPD_L0
		AR7	IFPD_L0*
		AR6	IFPD_L1
		AR5	IFPD_L1*
		AR4	IFPD_L2
		AR3	IFPD_L2*
		AR2	IFPD_L3
		AR1	IFPD_L3*
		AK4	IFPE_AUX_I2CY_SCL
		AK3	IFPE_AUX_I2CY_SDA*
		AK6	IFPE_L0
		AK5	IFPE_L0*
		AK4	IFPE_L1
		AK3	IFPE_L1*
		AK2	IFPE_L2
		AK1	IFPE_L2*
		AJ6	IFPE_L3
		AJ5	IFPE_L3*
		AK3	IFPF_AUX_I2CZ_SCL
		AK2	IFPF_AUX_I2CZ_SDA*
		AJ2	IFPF_L0
		AJ1	IFPF_L0*
		AJ3	IFPF_L1
		AJ2	IFPF_L1*
		AJ1	IFPF_L2
		AH1	IFPF_L2*
		AK2	IFPF_L3
		AK1	IFPF_L3*
AJ12	DACA_VDD	AM15	DACA_RED
		AM14	DACA_GREEN
		AL14	DACA_BLUE
AK12	DACA_VREF	AM13	DACA_HSYNC
AK13	DACA_RSET	AL13	DACA_VSYNC
AG7	DACB_VDD	AK4	DACB_RED
		AK3	DACB_GREEN
AK6	DACB_VREF	AK1	DACB_BLUE
AK7	DACB_RSET	AB5	CEC
AC6	IFPD_PLLVDD		
AB6	IFPD_RSET	AM1	DACB_HSYNC
		AM2	DACB_VSYNC

LVDS_EG_A_CLK_P
LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>
LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>
LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>
LVDS_EG_A_DATA_N<2>
NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_CLK_P
NC_LVDS_EG_B_CLK_N
LVDS_EG_B_DATA_P<0>
LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>
LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>
LVDS_EG_B_DATA_N<2>
NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>
DP_EG_AUX_CH_P
DP_EG_AUX_CH_N
DP_EG_ML_P<0>
DP_EG_ML_N<0>
DP_EG_ML_P<1>
DP_EG_ML_N<1>
DP_EG_ML_P<2>
DP_EG_ML_N<2>
DP_EG_ML_P<3>
DP_EG_ML_N<3>

NO STUFF
R8861 1K 5% 1/16W MF-LF 402

NO STUFF
R8860 1K 5% 1/16W MF-LF 402

81 PP1V1_GPU_IFPCD_IOVDD_F
81 PP1V1_GPU_IFPEF_IOVDD_F
81 GPU_IFPAB_RSET
81 PP3V3_GPU_IFPC_PLLVDD_F
81 GPU_IFPC_RSET
81 PP1V8_GPU_IFPEF_PLLVDD_F
81 GPU_IFPEF_RSET
84 85 LVDS_EG_DDC_CLK
84 85 LVDS_EG_DDC_DATA
85 NC_GPU_I2CC_SCL
85 NC_GPU_I2CC_SDA
97 51 48 45 SMBUS_SMC_0_S0_SCL
97 51 48 45 SMBUS_SMC_0_S0_SDA
85 NC_GPU_I2CH_SDA
85 NC_GPU_I2CH_SCL
84 85 DP_EG_DDC_CLK
84 85 DP_EG_DDC_DATA

GPU_DACA_VDD
GPU_DACB_VDD
PP1V8_GPU_IFPD_PLLVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

81 GPU_IFPD_RSET

PP3V3_S0GPU
6 7 72 74 79 80 81 82 84
R8859 10K 5% 1/16W MF-LF 402

GPU_CEC

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 VIDEO INTERFACES

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 88 OF 132
SHEET 81 OF 101

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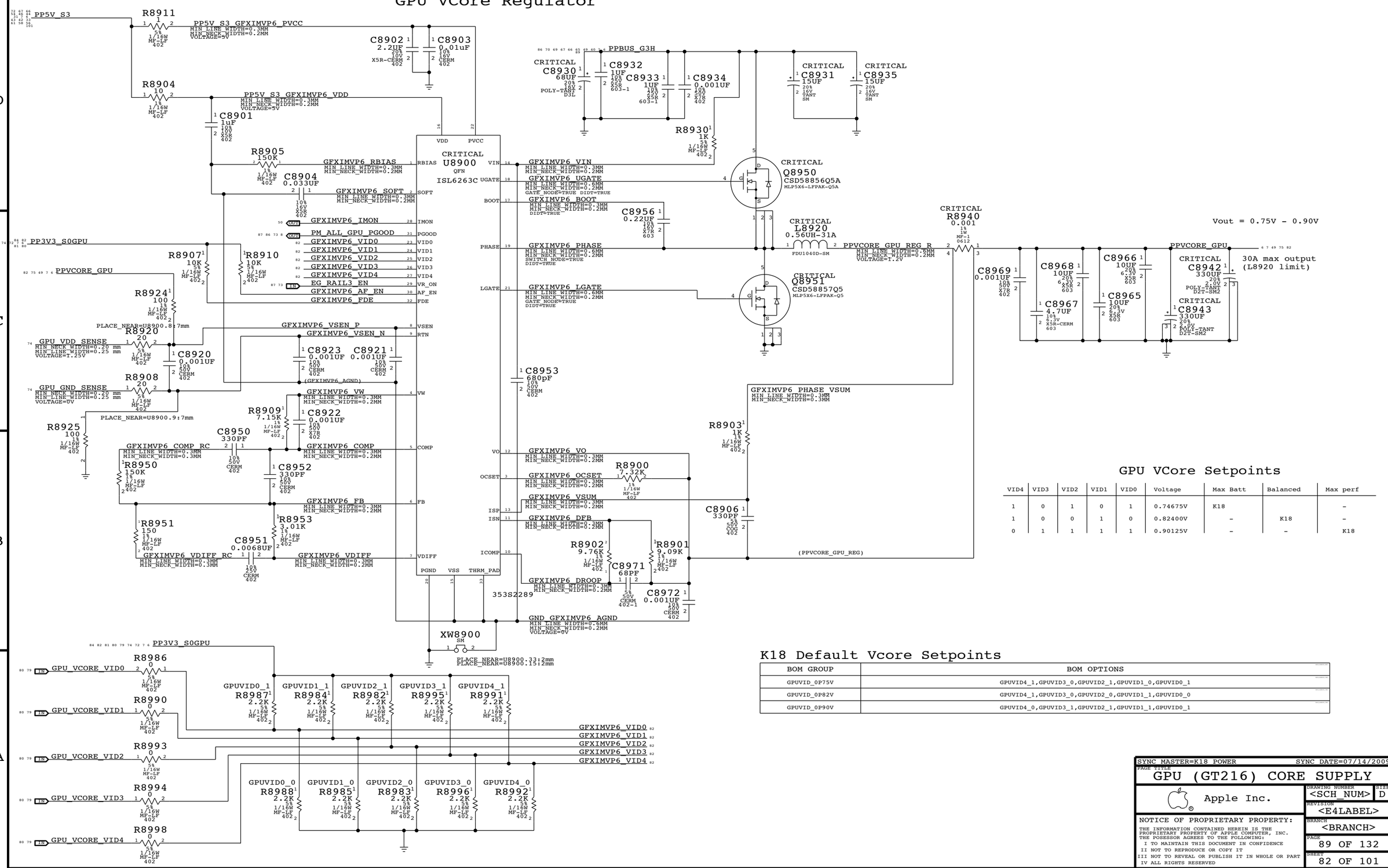
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

K18 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1,GPUVID3_0,GPUVID2_1,GPUVID1_0,GPUVID0_1
GPUVID_0P82V	GPUVID4_1,GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_0P90V	GPUVID4_0,GPUVID3_1,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC MASTER=K18 POWER SYNC DATE=07/14/2009

PAGE TITLE
GPU (GT216) CORE SUPPLY

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BRANCH <BRANCH>
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SHEET 82 OF 101

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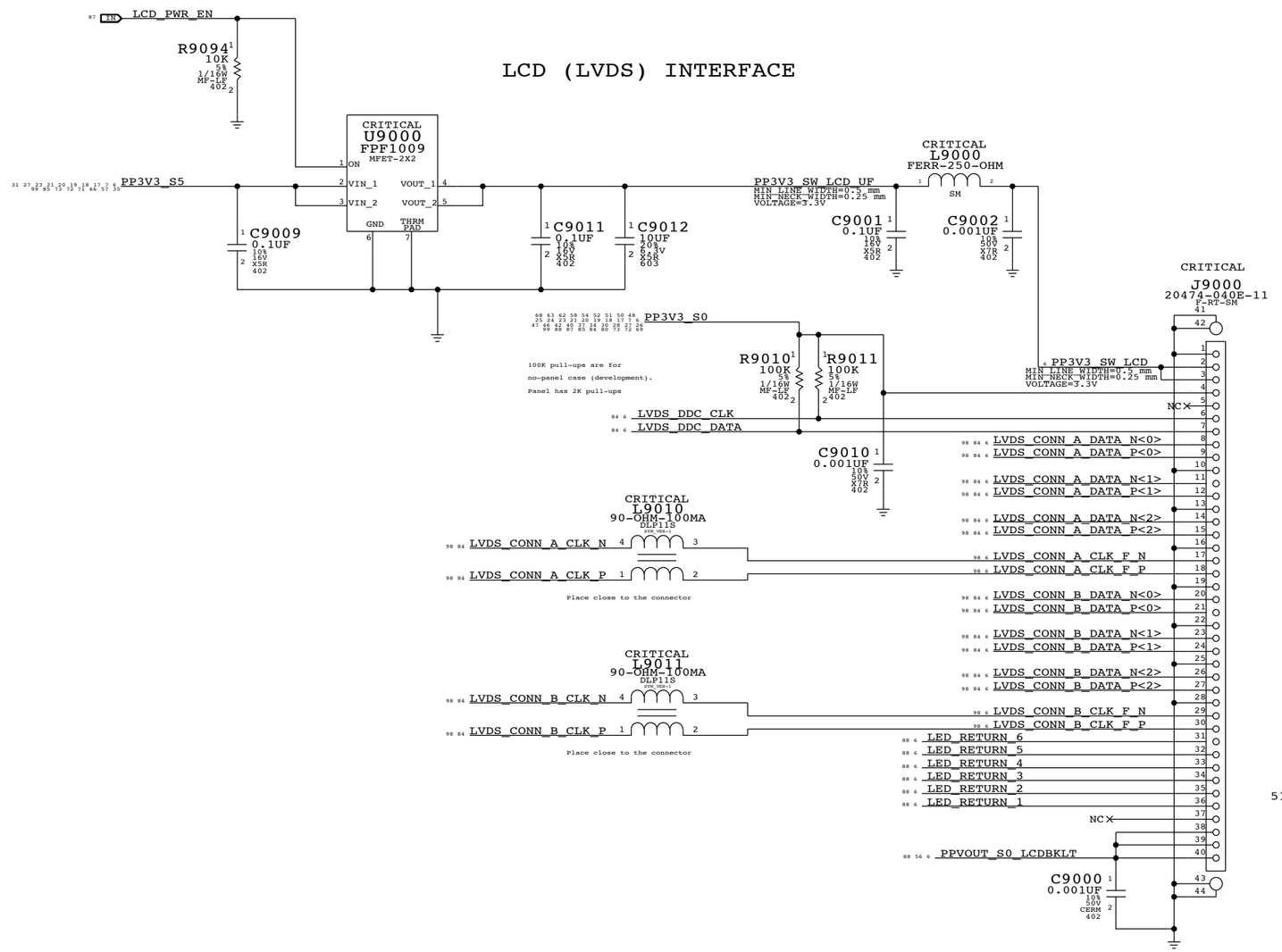
LCD (LVDS) INTERFACE



518S0651

SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE
LVDS Display Connector

Apple Inc.

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PAGE 90 OF 132

SHEET 83 OF 101

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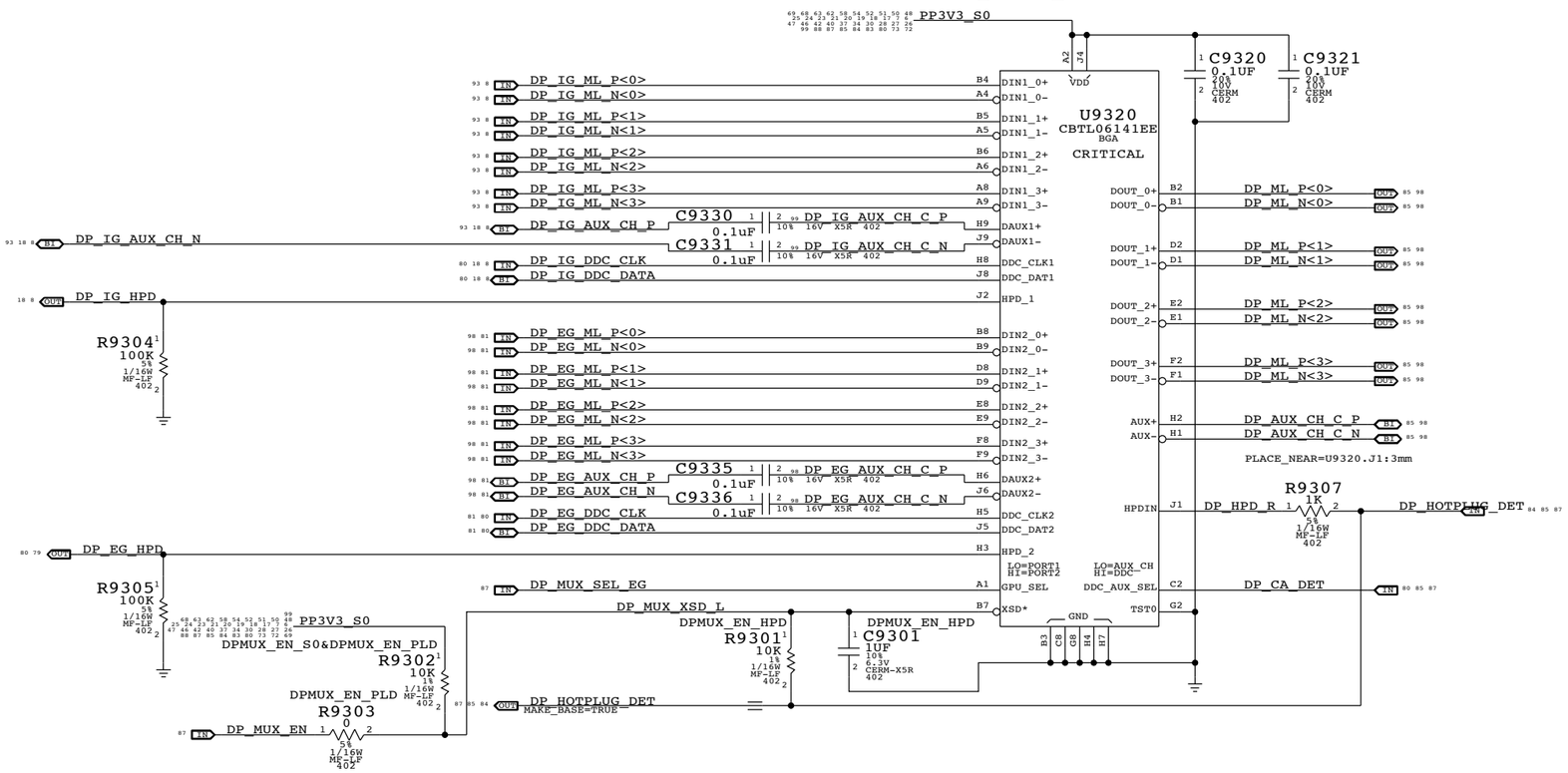
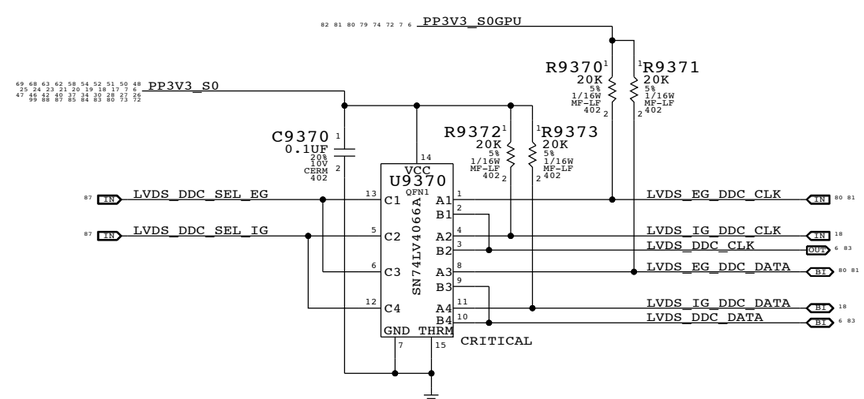
LVDS Transmitter Termination

All emulated LVDS outputs require this termination

DisplayPort Mux



LVDS DDC MUX



SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
Muxed Graphics Support

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PAGE 93 OF 132

SHEET 84 OF 101

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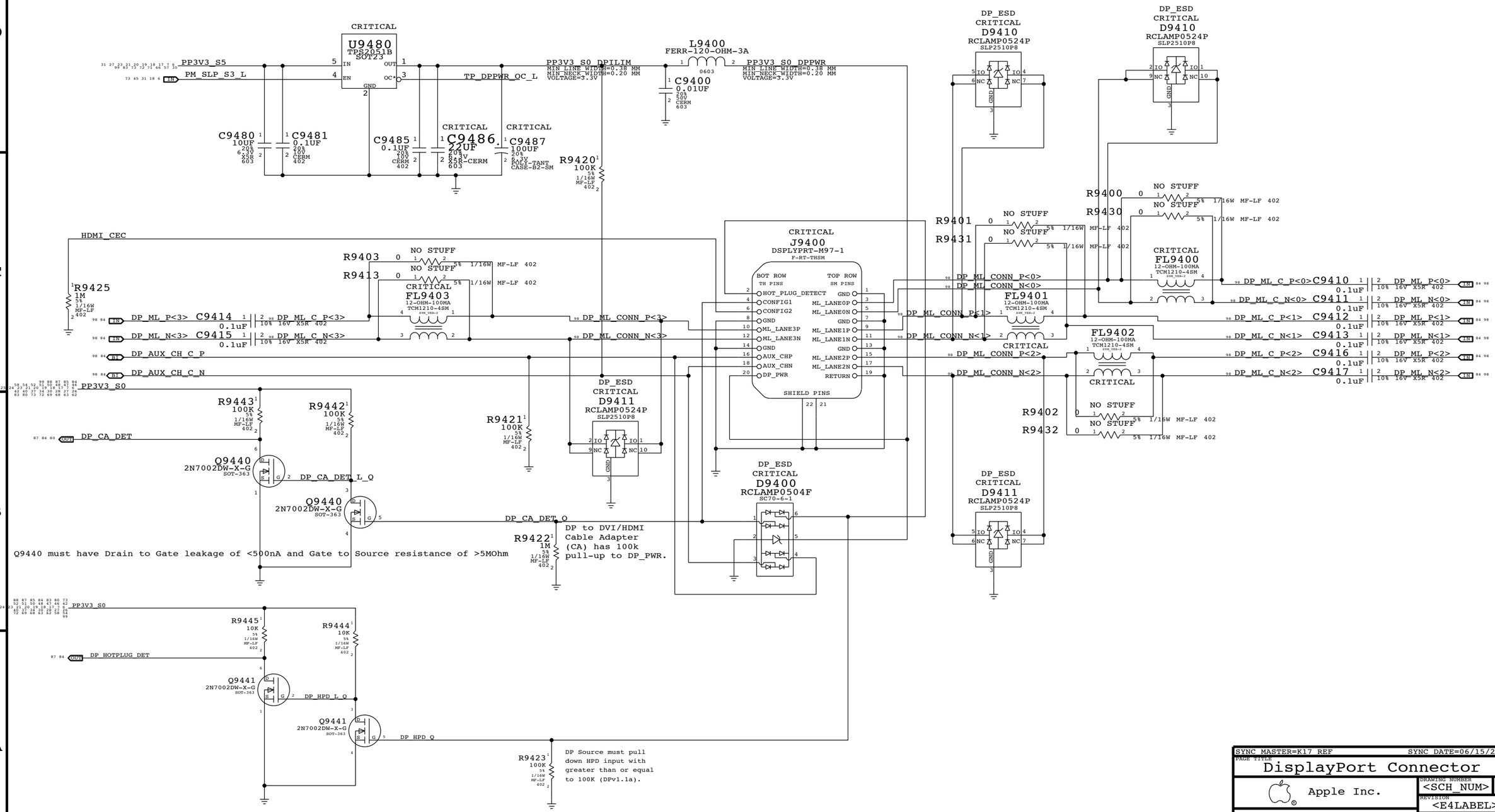
Port Power Switch



SYNC MASTER=K17_REF SYNC DATE=06/15/2009

PAGE TITLE
DisplayPort Connector

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DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE 94 OF 132

SHEET 85 OF 101

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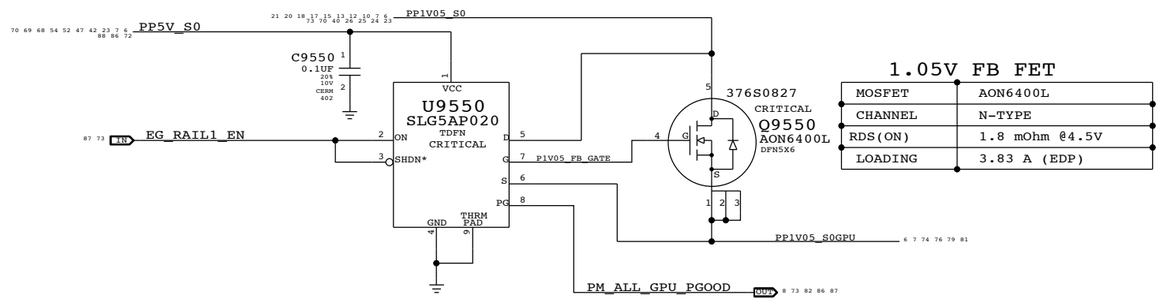
1V05 S0 GPU FET



1.05V FB FET

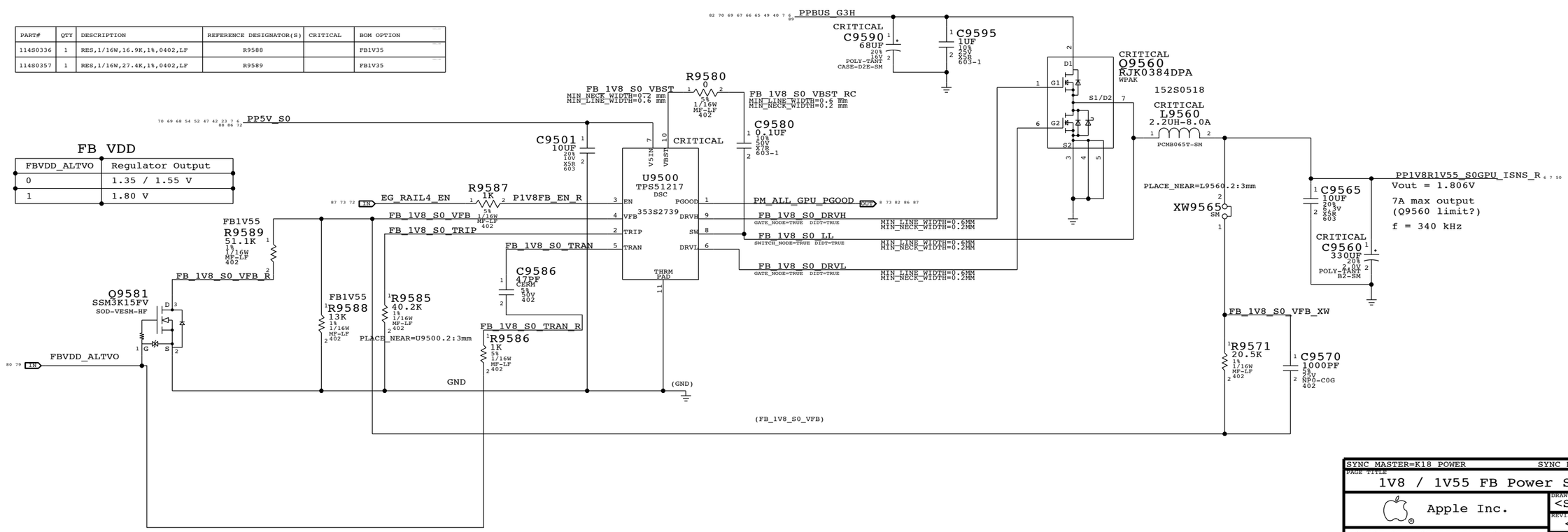
MOSFET	AON6400L
CHANNEL	N-TYPE
RDS(ON)	1.8 mOhm @4.5V
LOADING	3.83 A (EDP)

1V8 / 1V55 / 1V35 S0 FRAMEBUFFER REGULATOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0336	1	RES,1/16W,16.9K,1%,0402,LF	R9588		FB1V35
114S0357	1	RES,1/16W,27.4K,1%,0402,LF	R9589		FB1V35

FB_VDD

FBVDD_ALTVO	Regulator Output
0	1.35 / 1.55 V
1	1.80 V



SYNC MASTER=K18 POWER SYNC DATE=06/26/2009

PAGE TITLE
1V8 / 1V55 FB Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 95 OF 132

SHEET 86 OF 101

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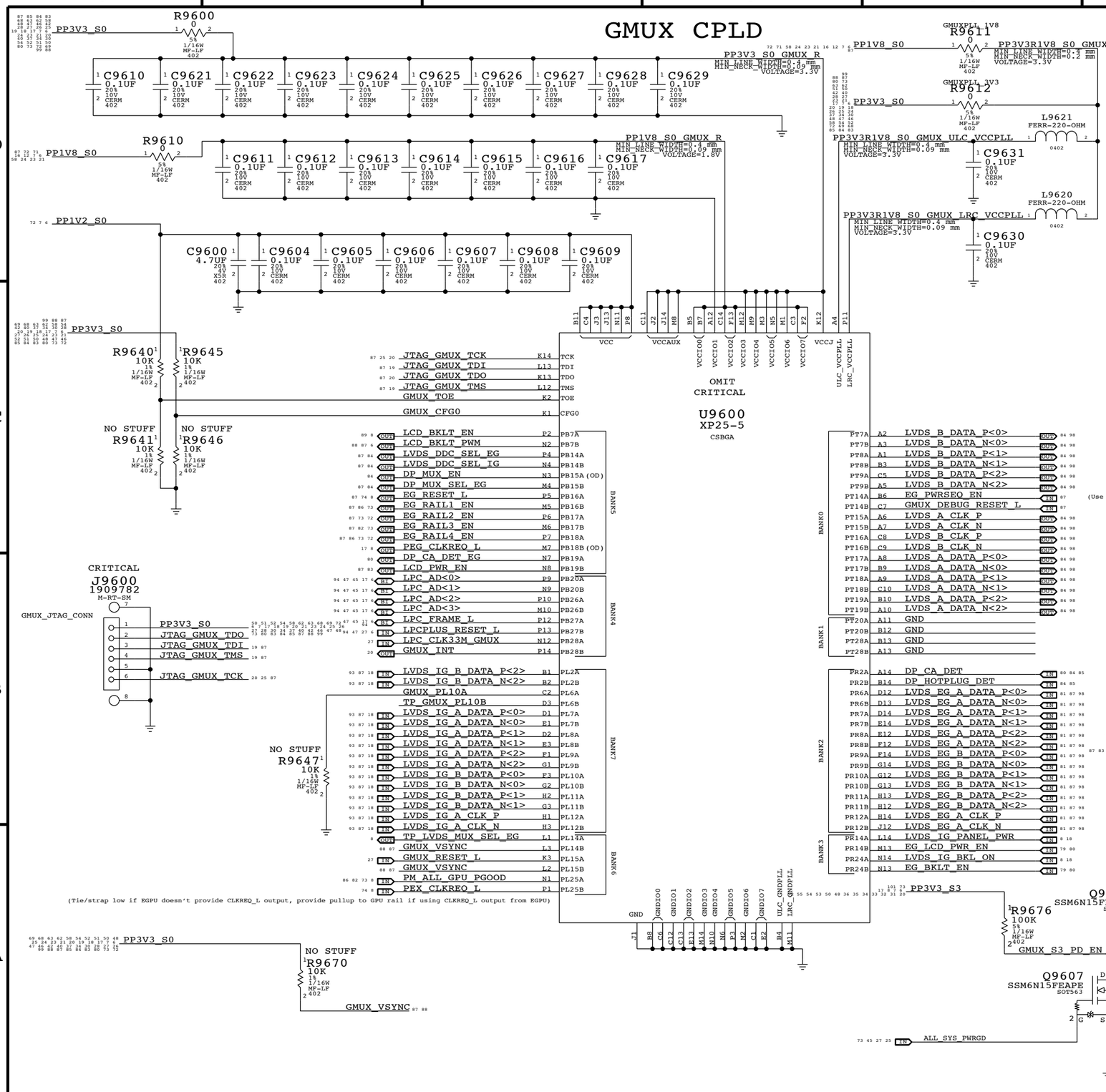
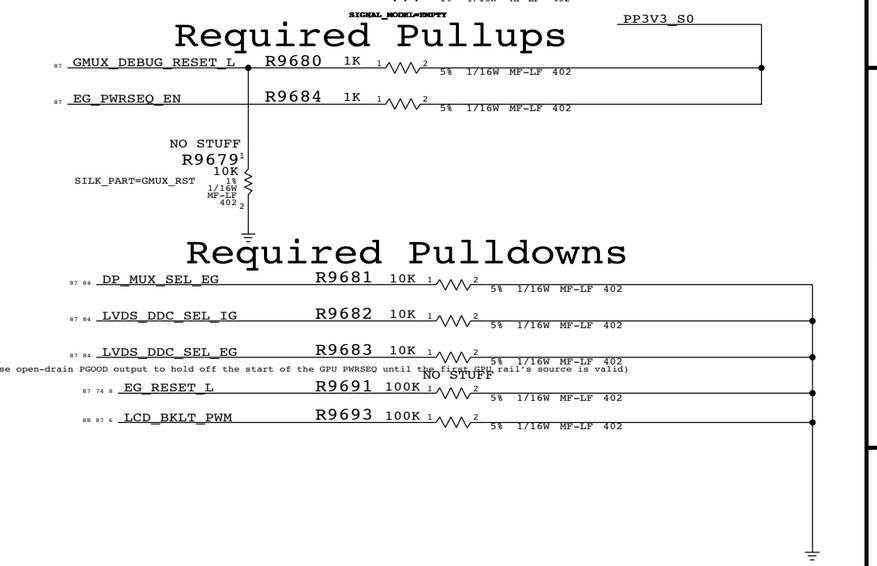
GMUX CPLD



LVDS Receiver Termination



Required Pullups

Required Pulldowns

SYNC MASTER=K17_REF	SYNC DATE=06/15/2009
PAGE TITLE: Graphics MUX (GMUX)	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 96 OF 132
	SHEET: 87 OF 101

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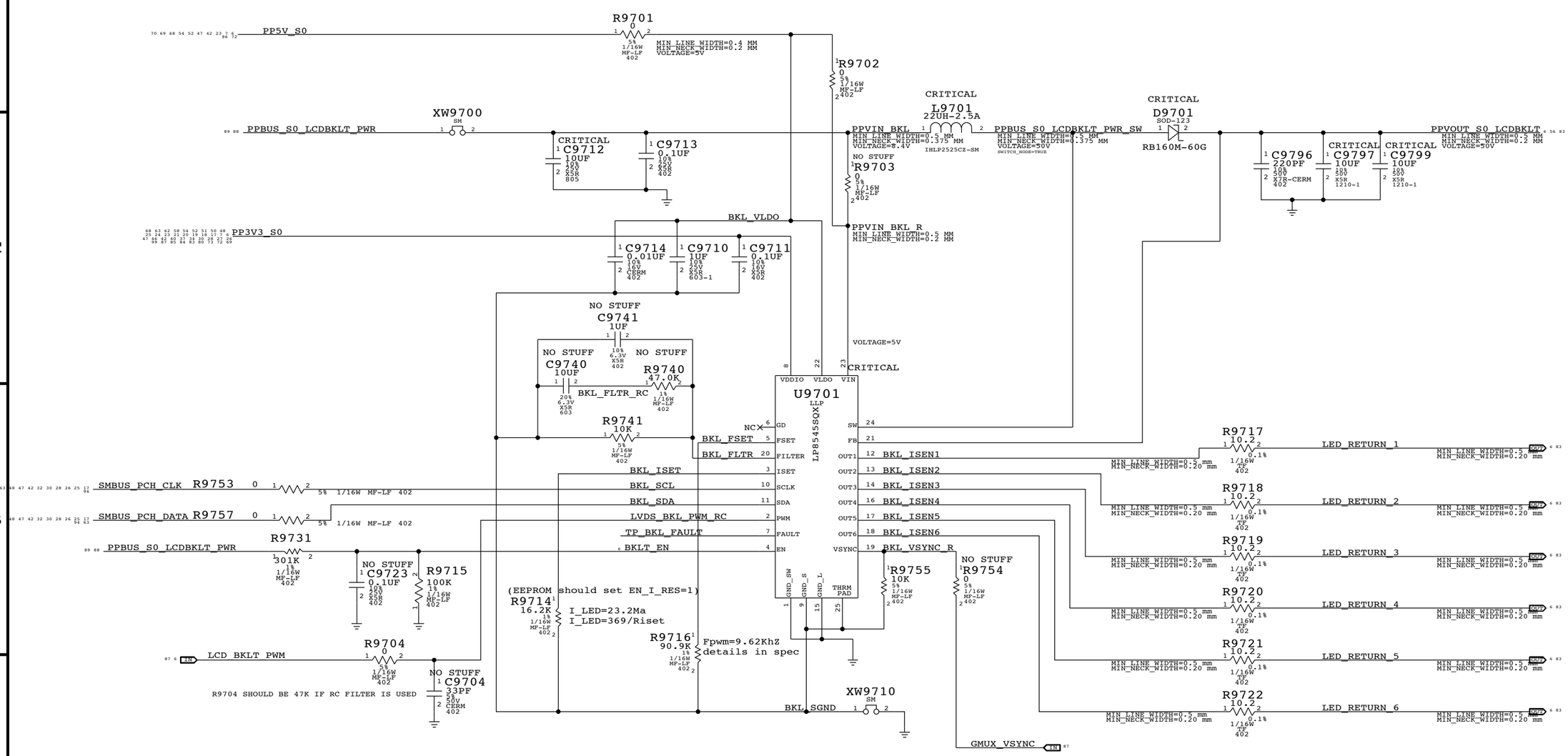
*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



SYNC MASTER=K18 BKLT SYNC DATE=07/29/2009

PAGE TITLE

LCD BACKLIGHT DRIVER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 97 OF 132

SHEET 88 OF 101

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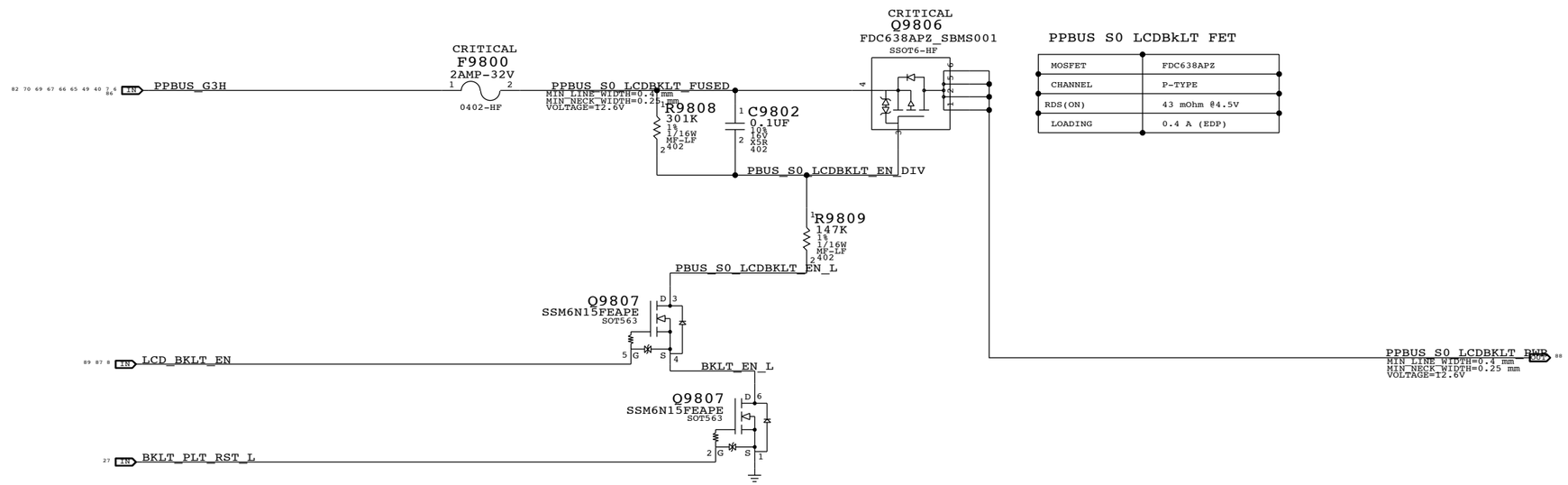
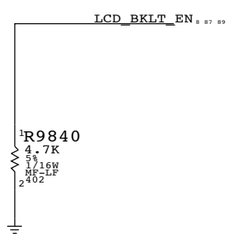


PPBUS_S0_LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)



SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

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PAGE 98 OF 132

SHEET 89 OF 101

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Blank Page, was 1.2V/1.8V in K19

SYNC MASTER=K18 POWER SYNC DATE=06/10/2009

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE 99 OF 132

SHEET 90 OF 101

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.1 and Table 4-184.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTS0_PGOOD	10 70
XDP_XPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 46
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 46
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 46
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 68
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	12 15 68
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 69
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	13 69
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 69
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 69
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	74

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
CPU Constraints

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DRAWING NUMBER <SCH_NUM> SIZE D
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PAGE 100 OF 132
SHEET 91 OF 101

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0>	11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4>	11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7>	11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 29 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0>	11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4>	11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 29

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
Memory Constraints

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 101 OF 132
SHEET 92 OF 101

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8 84
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 18 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 18 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 87
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAP<3>	8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAN<3>	8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 42
	SATA_90D	SATA	SATA_HDD_D2R_N	17 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	17 42
	SATA_90D	SATA	SATA_ODD_D2R_N	17 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	6 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N	42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N	42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	17
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	19 35
	USB_85D	USB	USB_HUB1_UP_N	19 35
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	19 36
	USB_85D	USB	USB_HUB2_UP_N	19 36
USB_EXTA	USB_85D	USB	USB_EXTA_P	36 43
	USB_85D	USB	USB_EXTA_N	36 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	35 43
	USB_85D	USB	USB_EXTB_N	35 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 35
	USB_85D	USB	USB_EXTC_N	8 35
USB_EXTD	USB_85D	USB	USB_EXTD_P	
	USB_85D	USB	USB_EXTD_N	
USB_MINI	USB_85D	USB	USB_MINI_P	
	USB_85D	USB	USB_MINI_N	
USB_WM	USB_85D	USB	USB_WM_P	
	USB_85D	USB	USB_WM_N	
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 33
	USB_85D	USB	USB_CAMERA_CONN_N	6 33
USB_BT	USB_85D	USB	USB_BT_P	33 36
	USB_85D	USB	USB_BT_N	33 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	36 53
	USB_85D	USB	USB_TPAD_N	36 53
USB_IR	USB_85D	USB	USB_IR_P	35 44
	USB_85D	USB	USB_IR_N	35 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	8 34 36
	USB_85D	USB	USB_SDCARD_N	8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	19 101
	USB_85D	USB	USB_BRCRYPT_N	19 101
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	19
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17 26
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17 26
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17 26
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
PCH Constraints 1

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REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 102 OF 132
SHEET 93 OF 101

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 45 47 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 45 47 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 47 87
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 58
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 58
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 58
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 58
	HDA_50S	HDA	AUD_SDI_R	58
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 58
	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 46
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 74
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 74
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 17
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 17
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20
123	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20
123	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20
124	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20
125	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
PCH Constraints 2

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PAGE 103 OF 132

SHEET 94 OF 101

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	27 37
	ENET_50S	ENET_3X	ENET_RESET_L	27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
Ethernet Constraints

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DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PAGE 104 OF 132

SHEET 95 OF 101

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 40 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 40 41
Port 2 Not Used				

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PAGE TITLE
FireWire Constraints

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PAGE 105 OF 132

SHEET 96 OF 101

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 33 45 48 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 33 45 48 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	45 48 51 81
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	45 48 51 81
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 64 65
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 64 65
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48 56
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48 56

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	65
	1TO1_DIFFPAIR		CHGR_CSI_N	65
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	65
	1TO1_DIFFPAIR		CHGR_CSO_N	65

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
SMC Constraints

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DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE 106 OF 132

SHEET 97 OF 101

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1149 LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	84 87
1147 LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	84 87
1158 LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	84 87
1156 LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	84 87
1153 LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	84 87
1151 LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	84 87
1203 LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	84 87
1205 LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	84 87
1182	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 83
1184	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 83
1186	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 83
1188	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 83
1180	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	83 84
1178	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	83 84
1177	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 83 84
1175	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 83 84
1194	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	83 84
1192	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	83 84
1190	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 83 84
1197	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 83 84
1146 DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_P<3..0>	85
1148	DP_85D	DISPLAYPORT	DP_ML_C_N<3..0>	85
1157 DP_ML	DP_85D	DISPLAYPORT	DP_ML_P<3..0>	84 85
1155	DP_85D	DISPLAYPORT	DP_ML_N<3..0>	84 85
1202 DP_ML	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>	85
1203	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>	85
1152 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_P	84 85
1150 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_N	84 85

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	76 77
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	76 77
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	76 77
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCAS_L	76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE	76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE	76 77
1203 FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L	76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	76 77
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	76 77
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	76 77
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	76 77
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	76 77
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	76 77
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	76 77
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	76 77
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	76 77
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	76 77
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	76 77
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	76 77
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	76 77
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	76 77
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	76 77
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	76 77
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	76 77
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	76 77
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	76 77
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	76 77
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	76 77
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	76 77
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	76 77
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	76 77
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	76 77
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	76 77
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	76 77
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	76 77
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	76 77
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	76 77
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	76 77
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	76 77
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	76 77
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	76 77
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	76 77

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOTSA)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	27 79 80
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	81 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	81 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	81 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	81 87
1209 LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	80 81
1207 LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	80 81
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	81 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	81 87
1208 LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	80 81
1206 LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	80 81
1142 DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_P<3..0>	81 84
1144 DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_N<3..0>	81 84
1145 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P	81 84
1143 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N	81 84
1135	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_P	84
1132	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_N	84

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	76 78
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	76 78
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	76 78
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCAS_L	76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE	76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE	76 78
1204 FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L	76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	76 78
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	76 78
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	76 78
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	76 78
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	76 78
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	76 78
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	76 78
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	76 78
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	76 78
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	76 78
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	76 78
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	76 78
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	76 78
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	76 78
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	76 78
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	76 78
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	76 78
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	76 78
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	76 78
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	76 78
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	76 78
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	76 78
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	76 78
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	76 78
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	76 78
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	76 78
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	76 78
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	76 78
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	76 78
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	76 78
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	76 78
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	76 78
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	76 78
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	76 78
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	76 78
1210 FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCAS_L	76 77
1211 FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCAS_L	76 78

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
GPU (GT216) CONSTRAINTS

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 107 OF 132
SHEET 98 OF 101

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
	SATA_90D	SATA	SATA_ODD_R2D_UF_P	42
	SATA_90D	SATA	SATA_ODD_R2D_UF_N	42
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	42
	SATA_90D	SATA	SATA_HDD_D2R_UF_P	42
	SATA_90D	SATA	SATA_HDD_D2R_UF_N	42
	SATA_90D	SATA	SATA_HDD_R2D_UF_P	42
	SATA_90D	SATA	SATA_HDD_R2D_UF_N	42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 79 80
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 79 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_N	50
	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	50 70
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	50 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	50
	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_N	69
	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_P	69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_N	50 69
	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_P	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_N	50
	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	50
	SENSE_1TO1_55S	SENSE	GPUISENS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	50 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	50 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	56
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	49
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	56
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	56
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	50
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	50
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	50

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 33
	1TO1_DIFFPAIR		CHGR_CSI_R_P	65
	1TO1_DIFFPAIR		CHGR_CSI_R_N	65
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 65
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 65
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 43
	USB_85D	USB	CONN_USB2_BT_P	6 33
	USB_85D	USB	CONN_USB2_BT_N	6 33
	USB_85D	USB	USB_LT2_P	6 43
	USB_85D	USB	USB_LT2_N	6 43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	84
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	84
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 61 62
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	6 7 17 18 19 20 21 23 27 31 35 57 64 71 72 73 83 85 90 91 92
		SB_POWER	PP3V3_S0	6 7 17 18 19 20 21 23 24 25 26 27 28 30 34 37 40 42 44 46 48
		SB_POWER	PP1V5_S3RS0	6 7 13 16 31 42 72 73 63 68 87
		GND	GND	55 74 77 80 88 83 85

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PAGE TITLE
Project Specific Constraints

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 108 OF 132
SHEET 99 OF 101

K18 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
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PAGE 109 OF 132

SHEET 100 OF 101

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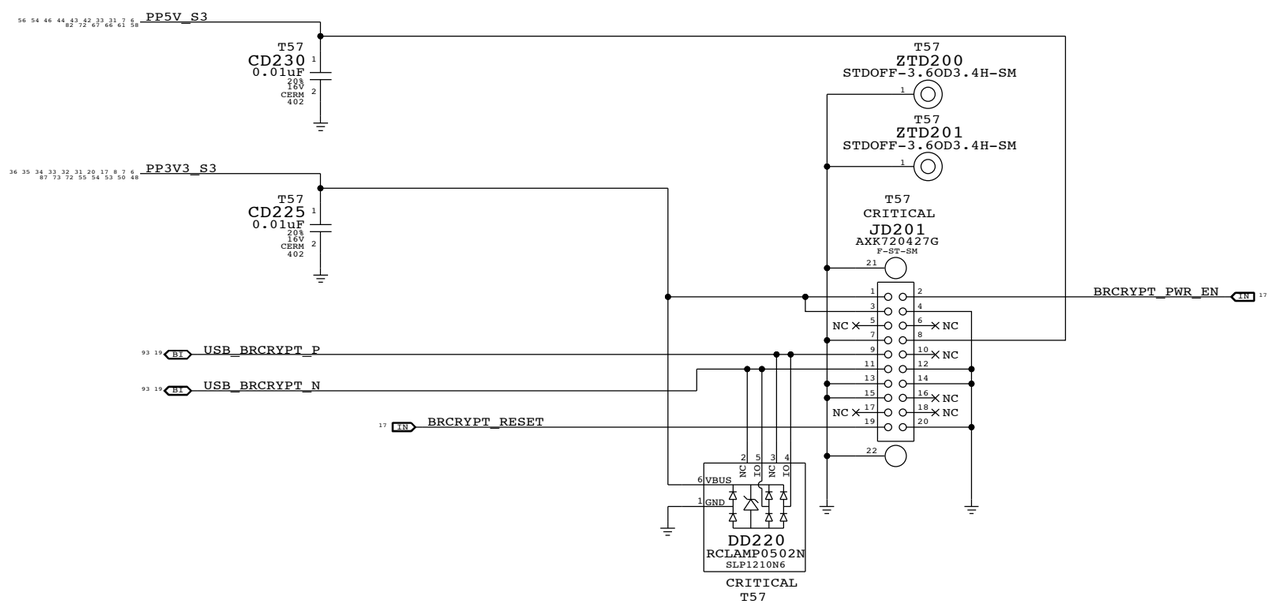

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PAGE TITLE

BluRay Decrypter Card Connector

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PAGE 132 OF 132

SHEET 101 OF 101

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